Sep. 2016

SCE18K1G160AF

1Gbit Mobile DDR ECC SDRAM

Data Sheet

Rev. A

Revision History		
Date	**Version**	**Subjects(major changes since last revision)**
2016-09	A	Initial Release Format Review (2020-05)

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1Gbit Mobile DDR ECC SDRAM
4 Banks X 16Mbit X 16

	5	6	75
	LPDDR400	LPDDR333	LPDDR266
Clock Cycle Time (t_{CK2})	12 ns	12 ns	12 ns
Clock Cycle Time (t_{CK3})	5 ns	6 ns	7.5 ns
Clock Cycle Time (t_{CK4})	5 ns	-	-
System Frequency (fCK)	200 MHz	166 MHz	133 MHz

Features

-Mobile DDR ECC SDRAM special architecture:
  2 bits Error Detect and 1 bit Correct for all DQs
  Long retention time for high reliability application
- 4 banks x 16M x 16 organization
- Data Mask for Write Control (DM)
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2, 3, 4
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  2, 4 or 8 for Sequential Type
  2, 4 or 8 for Interleave Type
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 8192 cycles/64ms
- Available in 60-ball BGA
- Double Data Rate (DDR)
- Bidirectional Data Strobe (DQS) for input and output data, active on both edges
- Differential clock inputs CLK and /CLK
- Power Supply 1.7V - 1.9V
- Auto Temperature-Compensated Self Refresh (Auto TCSR)
- Partial-Array Self Refresh (PASR) Option: Full, 1/2, 1/4
- Drive Strength (DS) Option:Full, 1/2, 1/4, 1/8

Option	*Marking*
- Configuration	
• 64Mx16 (4 Bank x16Mbit x16)	1G16
- Package	
• 60-ball FBGA (8mm x 10mm) Lead-free	F
- Speed/Cycle Time	
• 7.5ns @ CL3 (DDR-266)	-75B
• 6ns @ CL3(DDR-333)	-6B
• 5ns @ CL3 (DDR-400)	-5B
- Temperature	
• Commercial 0°C to 70°C Ta	<blank>
• Industrial -40°C to 85°C Ta	I
• Automotive -40°C to 105°C Ta	H

Description

The SCE18K1G160AFxx is a four bank mobile DDR ECC DRAM organized as 4 banks x 16M x 16. It achieves high speed data transfer rates by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock.

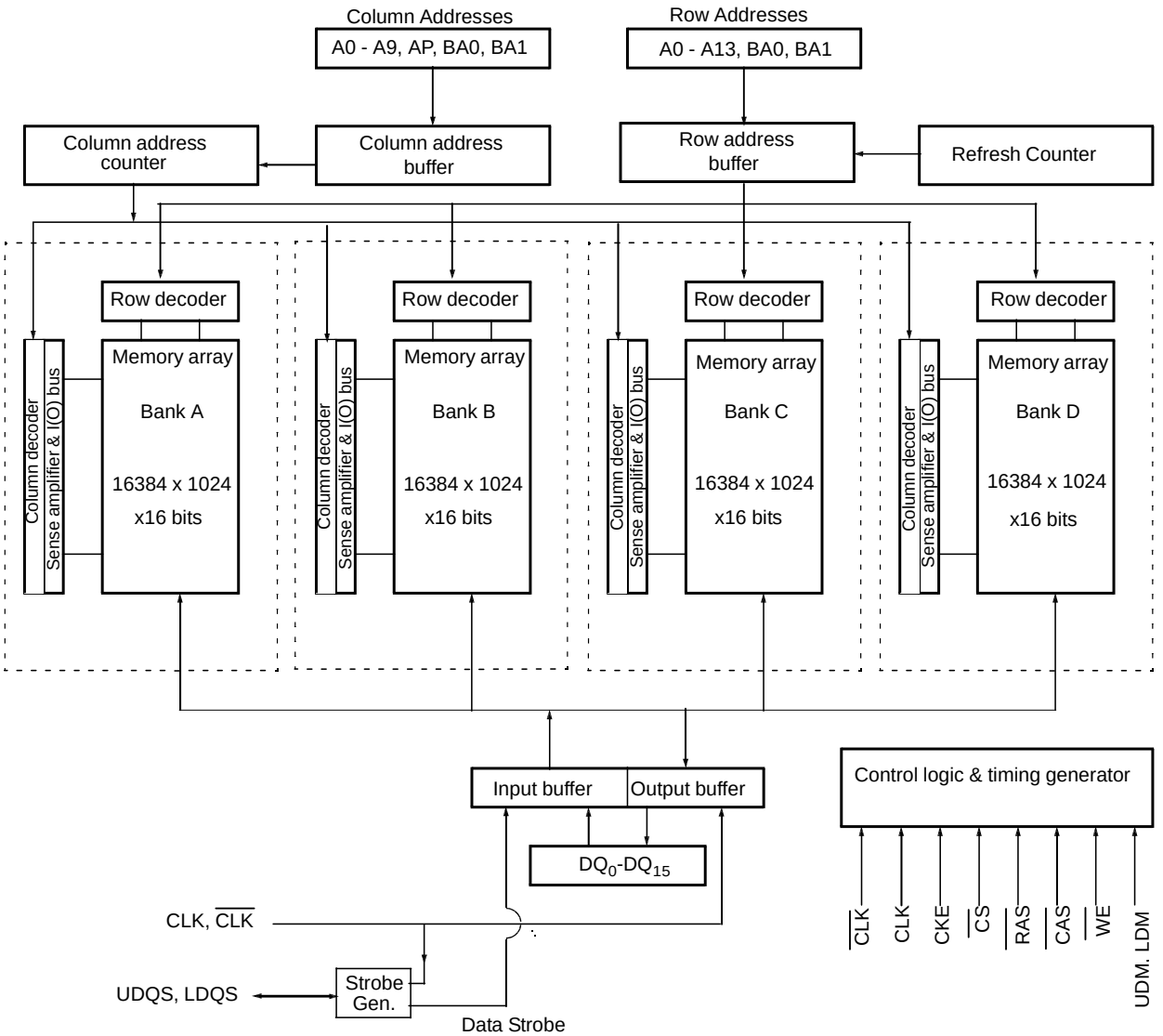
All of the control, address, circuits are synchronized with the positive edge of an externally supplied clock. I/O transactions are possible on both edges of DQS.
Operating the four memory banks in an interleaved fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Additionally, the device supports low power saving features like PASR, Auto-TCSR as well as options for different drive strength. It's ideally suitable for mobile application.

Product Type[1)]	Org.	Speed	CAS-RCD-RP Latencies[2)3)4)]	Clock (MHz)	Package	Note[5)]
Commercial Temperature Range (0 °C~ +70 °C)						
LPDDR-400 (3-3-3)						
SCE18K1G160AF-5B	×16	LPDDR-400B	3-3-3	200	PG-TFBGA-60	
LPDDR-333 (3-3-3)						
SCE18K1G160AF-6B	×16	LPDDR-333B	3-3-3	166	PG-TFBGA-60	
LPDDR-266 (3-3-3)						
SCE18K1G160AF-75B	×16	LPDDR-266B	3-3-3	133	PG-TFBGA-60	
Industrial Temperature Range (-40 °C~ +85 °C)						
LPDDR-400 (3-3-3)						
SCE18K1G160AF-5BI	×16	LPDDR-400B	3-3-3	200	PG-TFBGA-60	
LPDDR-333 (3-3-3)						
SCE18K1G160AF-6BI	×16	LPDDR-333B	3-3-3	166	PG-TFBGA-60	
LPDDR-266 (3-3-3)						
SCE18K1G160AF-75BI	×16	LPDDR-266B	3-3-3	133	PG-TFBGA-60	

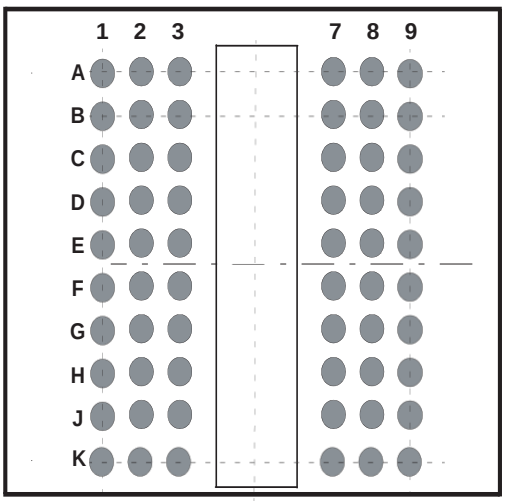
1) For detailed information regarding product type of UniIC please see chapter "Product Nomenclature" of this data sheet.
2) CAS: Column Address Strobe
3) RCD: Row Column Delay
4) RP: Row Precharge
5) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit **http://www.unisemicon.com/**

Block Diagram



60 BALL BGA CONFIGURATION

Top View



60Ball(6x10) CSP						
	1	**2**	**3**	**7**	**8**	**9**
A	V_{SS}	DQ15	V_{SSQ}	V_{DDQ}	DQ0	V_{DD}
B	V_{DDQ}	DQ13	DQ14	DQ1	DQ2	V_{SSQ}
C	V_{SSQ}	DQ11	DQ12	DQ3	DQ4	V_{DDQ}
D	V_{DDQ}	DQ9	DQ10	DQ5	DQ6	V_{SSQ}
E	V_{SSQ}	UDQS	DQ8	DQ7	LDQS	V_{DDQ}
F	V_{SS}	UDM	NC	A13	LDM	V_{DD}
G	CKE	CK	$\overline{CK}$	$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12	$\overline{CS}$	BA0	BA1
J	A6	A7	A8	A10/AP	A0	A1
K	V_{SS}	A4	A5	A2	A3	V_{DD}

Pin Names

CLK, $\overline{CLK}$	Differential Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
LDQS, UDQS	Data Strobe (Bidirectional)
A_0–A_{13}	Address Inputs
BA0, BA1	Bank Select

DQ_0–DQ_{15}	Data Input/Output
LDM, UDM	Data Mask
V_{DD}	Power (1.7V - 1.9V)
V_{SS}	Ground
V_{DDQ}	Power for I/O's (1.7V - 1.9V)
V_{SSQ}	Ground for I/O's

Signal Pin Description

Symbol	Type	Description
CK, $\overline{CK}$	Input	Clock: CK and CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/CK.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
CS	Input	Chip Select: CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
RAS, CAS, $\overline{WE}$	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.
LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. For x16 devices, LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0-A13	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
DQ, DQ0-DQ15	I/O	Data Bus: Input / Output
LDQS,UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. For x16 device, LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15.
NC	—	No Connect: No internal electrical connection is present
VDDQ	Supply	I/O Power Supply
VSSQ	Supply	I/O Ground
VDD	Supply	Power Supply
VSS	Supply	Ground

Mode Register Set

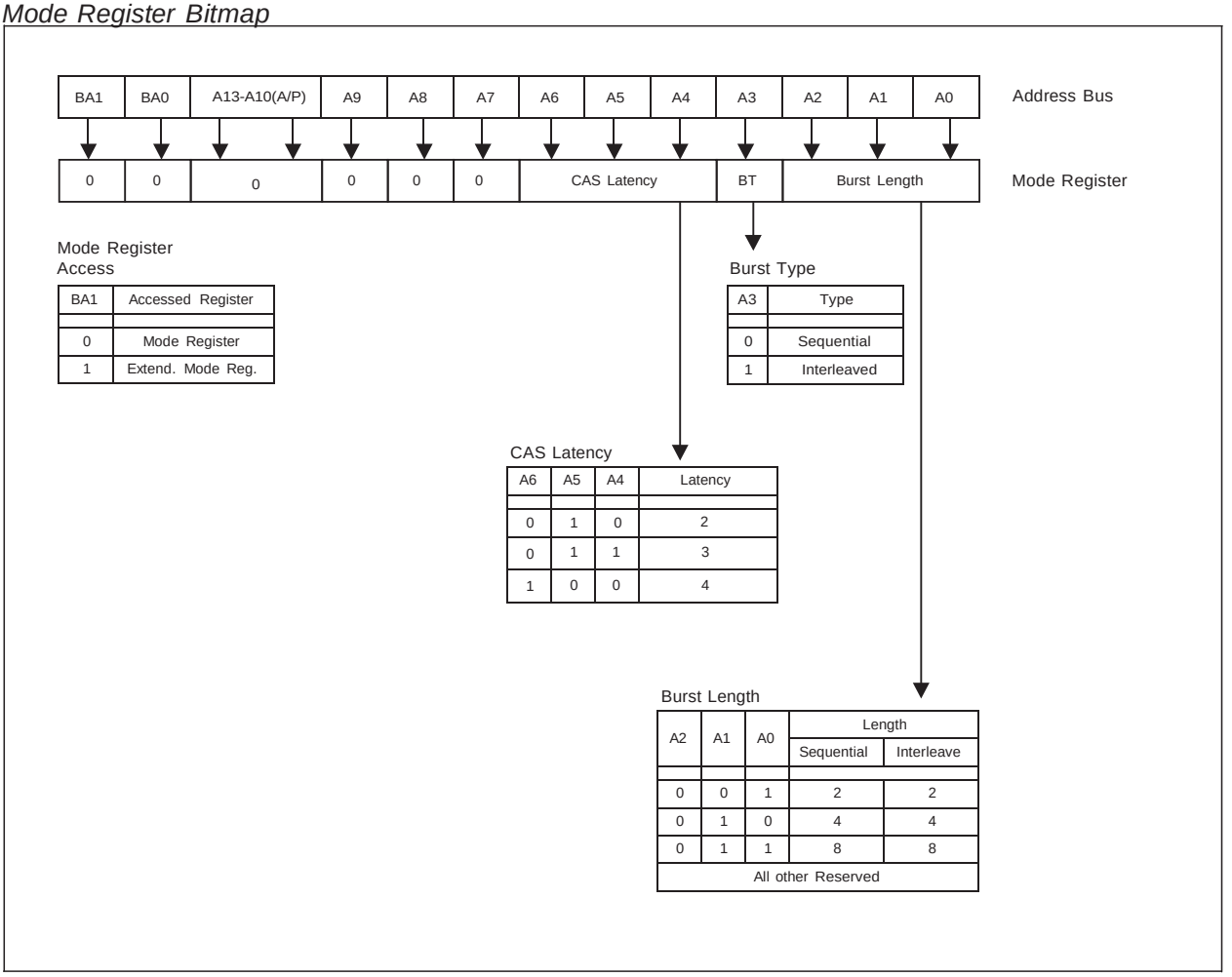
The mode register stores the data for controlling the various operating modes of the mobile DDR, includes CAS latency, addressing mode, burst length, test mode, and various vendor specific options. The default value of the mode register is not defined. Therefore the mode register must be written after power up to operate the mobile DDR. The device should be activated with the CKE already high prior to writing into the Mode Register.

The Mode Register is written by using the MRS command. The state of the address signals registered in the same cycle as MRS command is written in the mode register. The value can be changed as long as all banks are in the idle state.

The mode register is divided into various fields depending on functionality. The burst length uses A2.. A0, CAS latency (read latency from column address) uses A6.. A4. BA0 must be set to low for normal operation. A9.. A13 is reserved for future use.

BA1 selects Extended Mode Register Setup operation when set to 1. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.

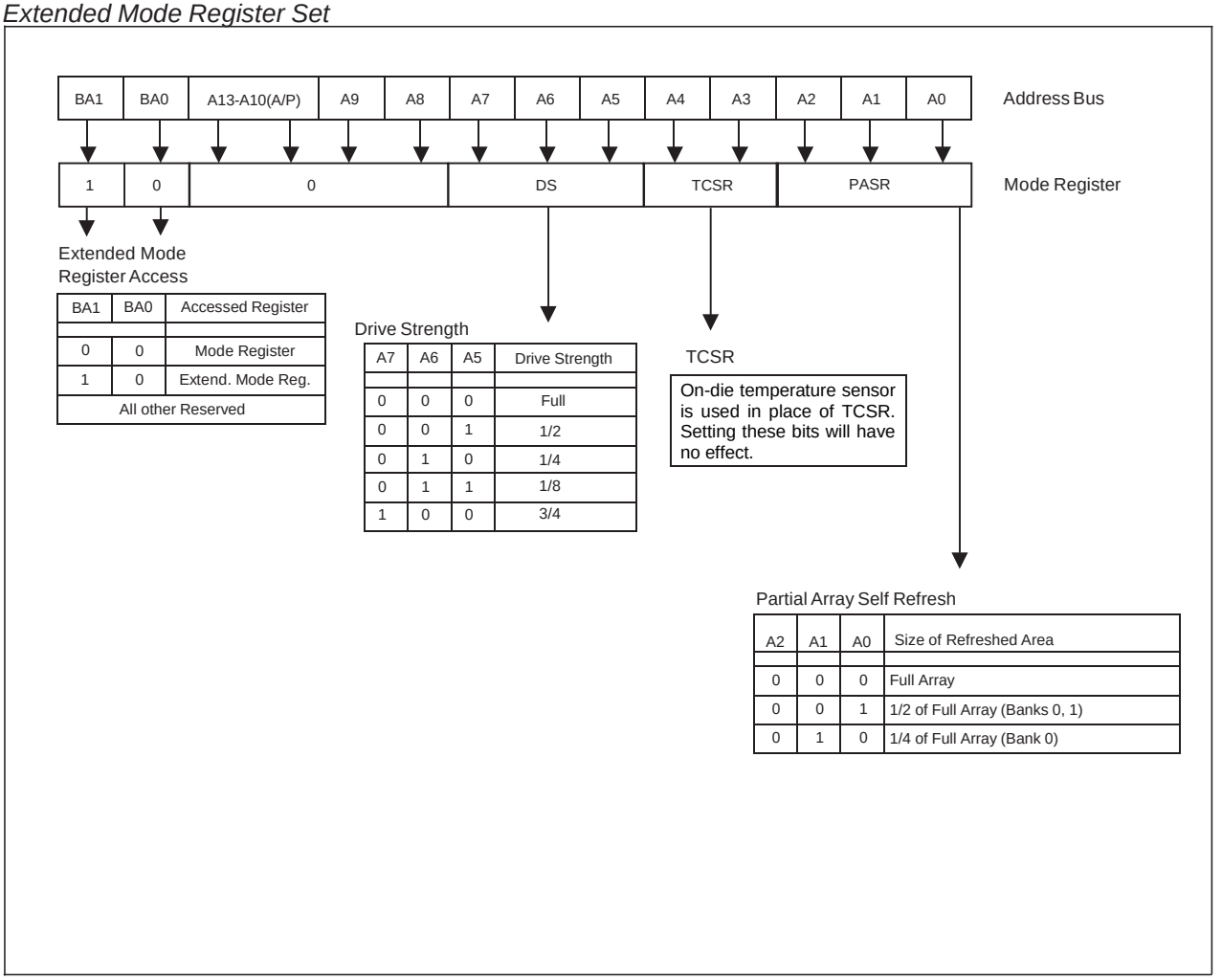
Mode Register Bitmap



EMRS

The Extended Mode Register is responsible for setting the Drive strength options and Partial array Self Refresh. The EMRS can be programmed by performing a normal Mode Register Setup operation and setting the BA1=1 and BA0=0. In order to save power consumption, the mobile DDR SDRAM has three (PASR) options: Full array, 1/2, 1/4 of Full Array. Additionally, the device has internal temperature sensor to control self refresh cycle automatically. This is the device internal Temperature Compensated Self Refresh(TCSR). The device has four drive strength options: Full, 1/2, 1/4 or 1/8.

Extended Mode Register Set



BA1	BA0	Accessed Register
0	0	Mode Register
1	0	Extend. Mode Reg.
All other Reserved		

A7	A6	A5	Drive Strength
0	0	0	Full
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	3/4

A2	A1	A0	Size of Refreshed Area
0	0	0	Full Array
0	0	1	1/2 of Full Array (Banks 0, 1)
0	1	0	1/4 of Full Array (Bank 0)

Signal and Timing Description

General Description

The 1G bit mobile DDR is a 128M byte mobile DDR SDRAM. It consists of four banks. Each bank is organized as 16384 rows x 1024 columns x 16 bits.

Read and Write accesses are burst oriented. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate command are used to select the bank and the row to be accessed. BA1 and BA0 select the bank, address bits A13.. A0 select the row. Address bits A9.. A0 registered coincident with the Read or Write command are used to select the starting column location for the burst access.

The regular Single Data Rate SDRAM read and write cycles only use the rising edge of the external clock input. For the mobile SDRAM the special signals DQSx (Data Strobe) are used to mark the data valid window. During read bursts, the data valid window coincides with the high or low level of the DQSx signals. During write bursts, the DQSx signal marks the center of the valid data window. Data is available at every rising and falling edge of DQSx, therefore the data transfer rate is doubled.

For Read accesses, the DQSx signals are aligned to the clock signal CLK.

Special Signal Description

Clock Signal

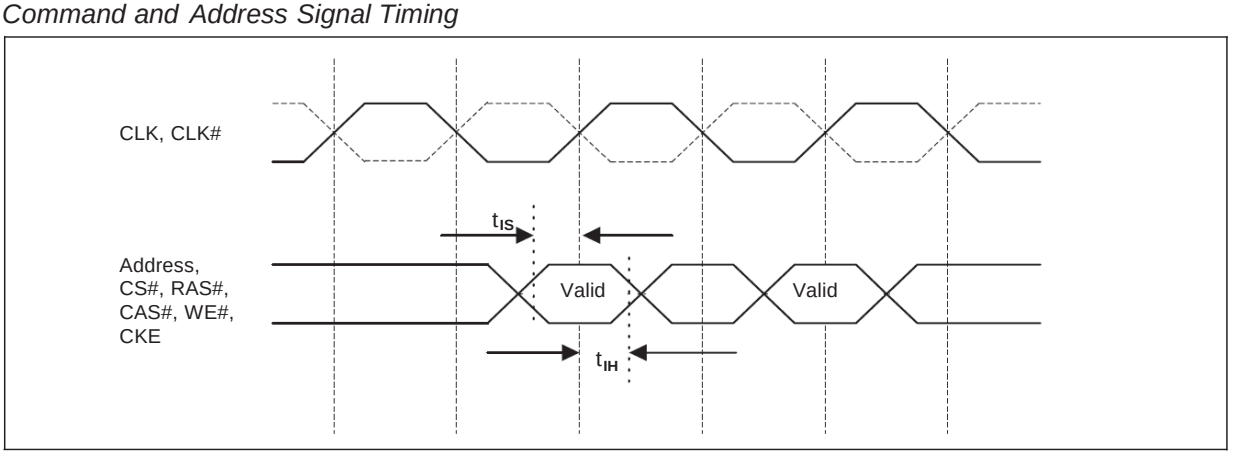
The mobile DDR operates with a differential clock ($\overline{CLK}$ and CLK) input. CLK is used to latch the address and command signals. Data input and DMx signals are latched with DQSx. The minimum and maximum clock cycle time is defined by t_{CK}.

The minimum and maximum clock duty cycle are specified using the minimum clock high time t_{CH} and the minimum clock low time t_{CL} respectively.

Command Inputs and Addresses

Like single data rate SDRAMs, each combination of $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the clock determines a mobile DDR command.

Command and Address Signal Timing



Data Strobe and Data Mask

Operation at Burst Reads

The Data Strobes provide a 3-state output signal to the receiver circuits of the controller during a read burst. The data strobe signal goes 1 clock cycle low before data is driven by the mobile DDR and then toggles low to high and high to low till the end of the burst. CAS latency is specified to the first low to high transition. The edges of the Output Data signals and the edges of the data strobe signals during a read are nominally coincident with edges of the input clock.

The tolerance of these edges is specified by the parameters t_{AC} and t_{DQSCK} and is referenced to the crossing point of the CLK and /CLK signal. The t_{DQSQ} timing parameter describes the skew between the data strobe edge and the output data edge.

The following table summarizes the mapping of LDQS, UDQS, LDM and UDM signals to the data bus.

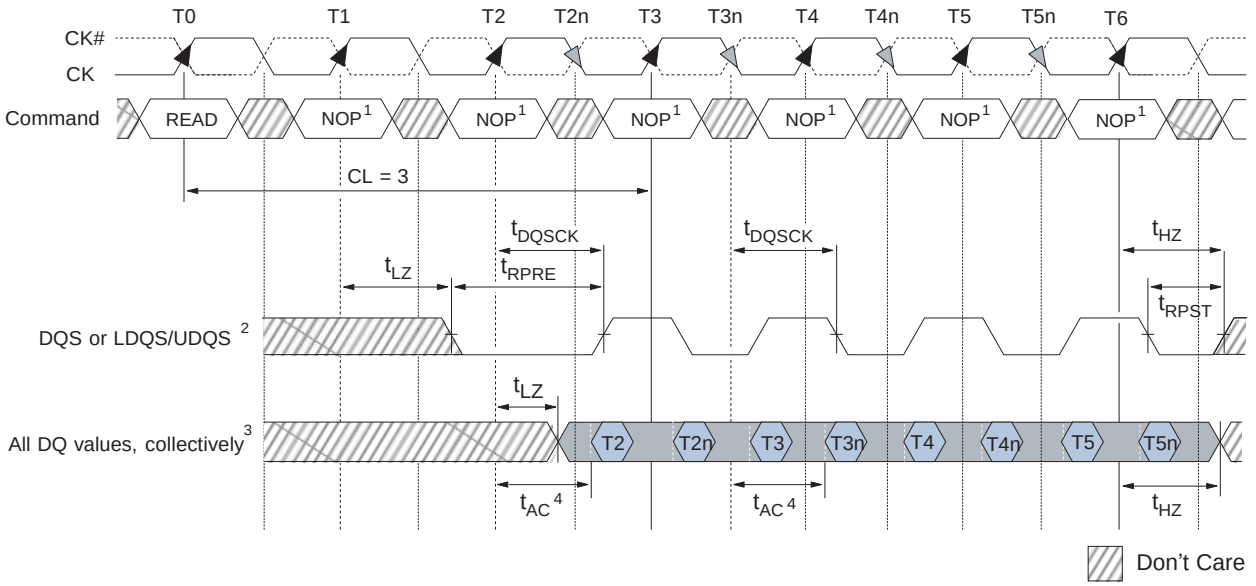
Mapping of LDQS, UDQS, LDM and UDM

Data strobe signal	Data mask signal	Controlled data bus
LDQS	LDM	DQ7 .. DQ0
UDQS	UDM	DQ8 .. DQ15

The minimum time during which the output data is valid is critical for the receiving device. This also applies to the Data Strobe DQS during a read since it is tightly coupled to the output data. The parameters t_{QH} and t_{DQSQ} define the minimum output data valid window. Prior to a burst of read data, given that the device is not currently in burst read mode, the data strobe signals transit from Hi-Z to a valid logic low. This is referred to as the data strobe “read preamble” t_{RPRE}. This transition happens one clock prior to the first edge of valid data.

Once the burst of read data is concluded, given that no subsequent burst read operation is initiated, the data strobe signals transit from a valid logic low to Hi-Z. This is referred to as the data strobe “read postamble” t_{RPST}.

Data Output Timing - t_{AC} and t_{DQSCK}



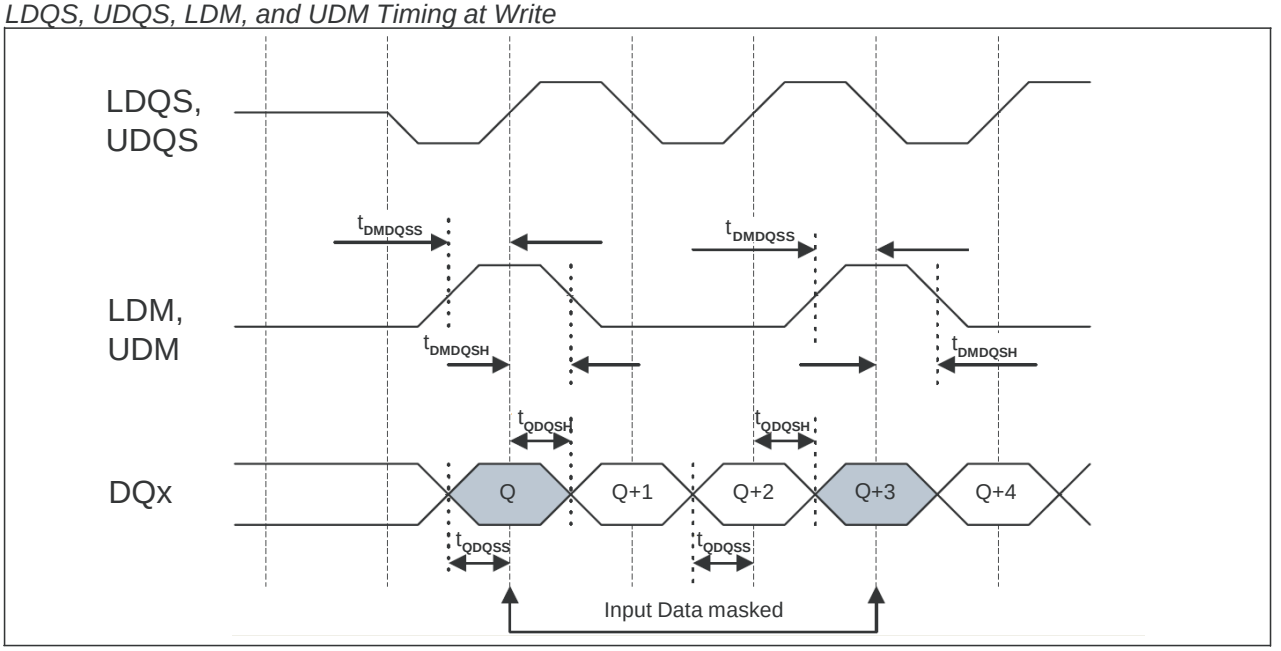
Notes:

1. Commands other than NOP can be valid during this cycle.
2. DQ transitioning after DQS transitions define t_{DQSQ} window.
3. All DQ must transition by t_{DQSQ} after DQS transitions, regardless of t_{AC}.
4. t_{AC} is the DQ output window relative to CK and is the long-term component of DQ skew.

Operation at Burst Write

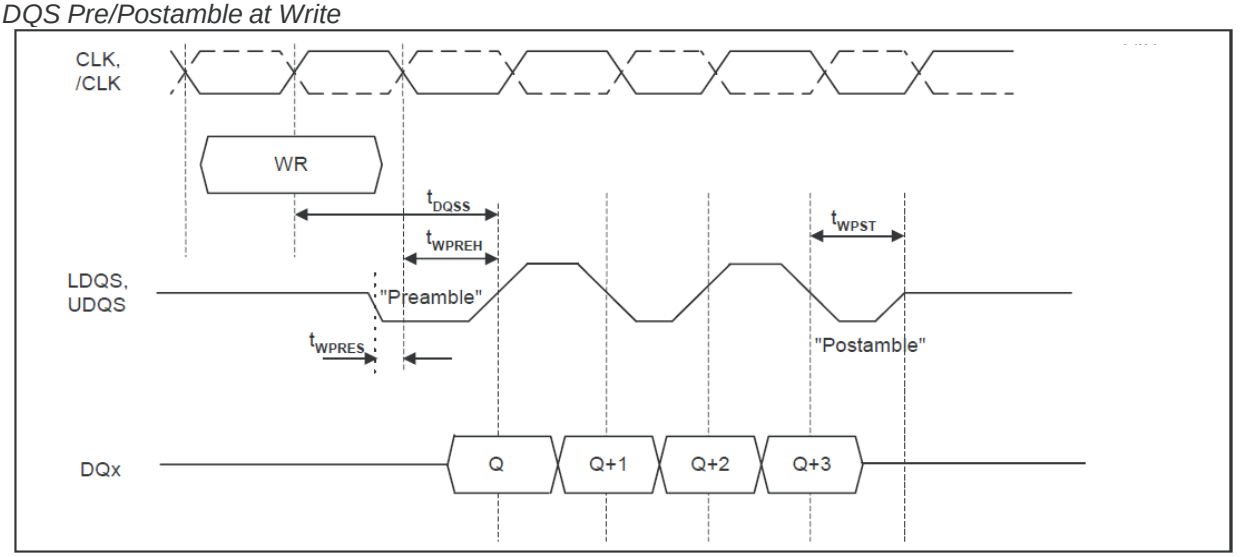
During a write burst, control of the data strobe is driven by the memory controller. The LDQS, UDQS signals are centered with respect to data and data mask. The tolerance of the data and data mask edges versus the data strobe edges during writes are specified by the setup and hold time parameters of data (tQDQSS & tQDQSH) and data mask (tDMDQSS & tDMDQSH). The input data is masked in the same cycle when the corresponding LDM, UDM signal is high (i.e. the LDM,UDM mask to write latency is zero.)

LDQS, UDQS, LDM, and UDM Timing at Write



Prior to a burst of write data, given that the controller is not currently in burst write mode, the data strobe signal LDQS, UDQS changes from Hi-Z to a valid logic low. This is referred to as the data strobe Write Preamble. Once the burst of write data is concluded, given no subsequent burst write operation is initiated, the data strobe signal LDQS,UDQS transits from a valid logic low to Hi-Z. This is referred the data strobe W rite Postamble, t_{WPST}. For mobile DDR data is written with a delay which is defined by the parameter t_{DQSS}, write latency). This is different than the single data rate SDRAM where data is written in the same cycle as the Write command is issued.

DQS Pre/Postamble at Write

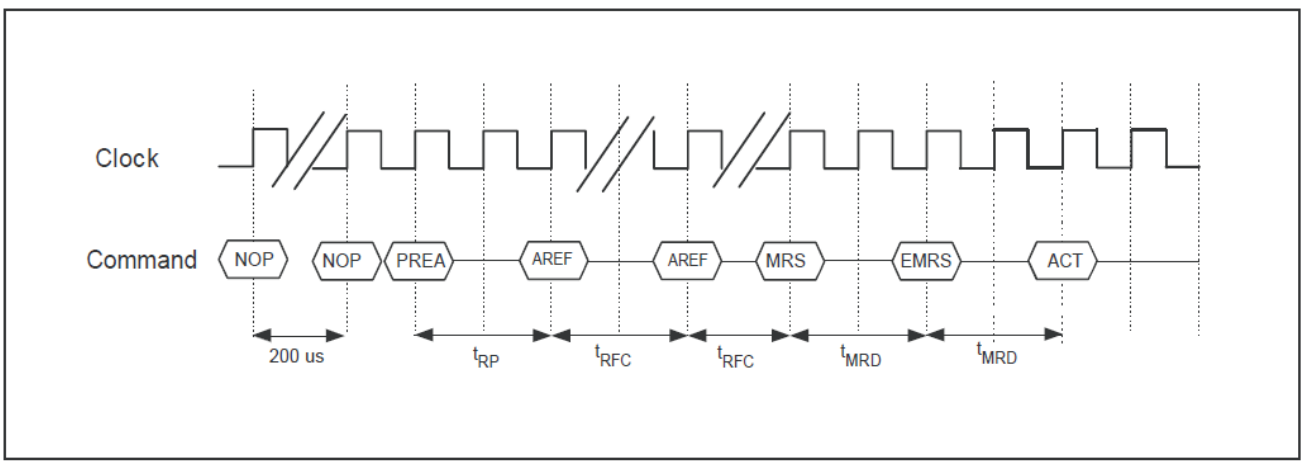


Power-Up Sequence

The following sequence is highly recommended for Power-Up:

1. Apply power and start clock. Maintain CKE and the other pins are in NOP conditions at the input
2. Apply V_{DD} before or at the same time as V_{DDQ}
3. Start clock, maintain stable conditions for 200 us
4. Apply NOP and set CKE to high
5. Apply All Bank Precharge command
6. Issue Auto Refresh command twice and must satisfy minimum t_{RFC}
7. Issue MRS (Mode Register Set command)
8. Issue a EMRS (Extended Mode Register Set command), not necessary

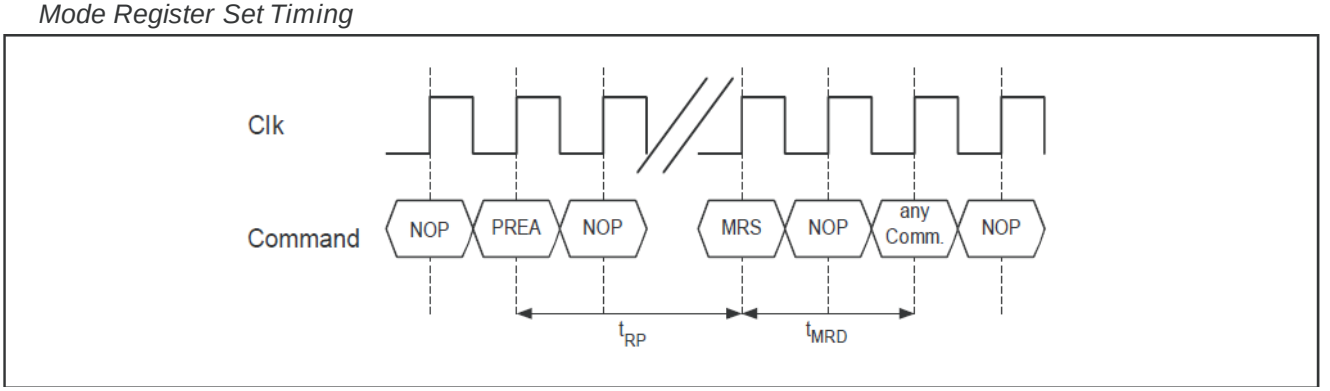
Power Up Sequence



Mode Register Set Timing

The mobile DDR should be activated with CKE already high prior to writing into the mode register. Two clock cycles are required complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state.

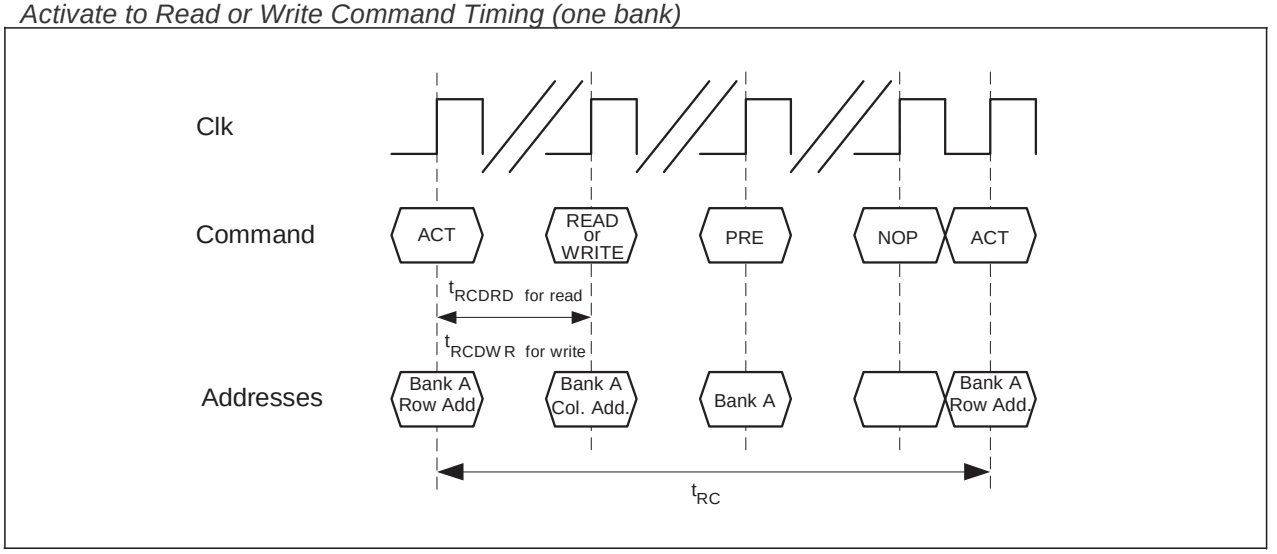
Mode Register Set Timing



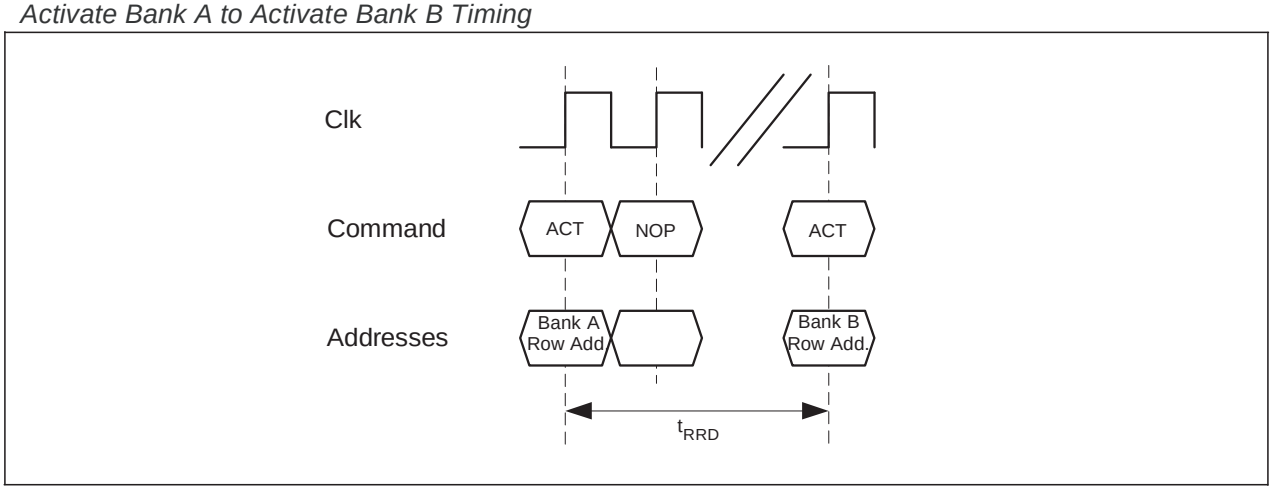
Bank Activation Command (ACT)

The Bank Activation command is initiated by issuing an ACT command at the rising edge of the clock. The mobile DDR has 4 independent banks which are selected by the two Bank select Addresses (BA0, BA1). The Bank Activation command must be applied before any Read or Write operation can be executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of RAS to CAS delay time (t_{RCDRD} min. for read commands and t_{RCDWR} min. for write commands). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank activation delay time (t_{RRD} min).

Activate to Read or Write Command Timing (one bank)



Activate Bank A to Activate Bank B Timing



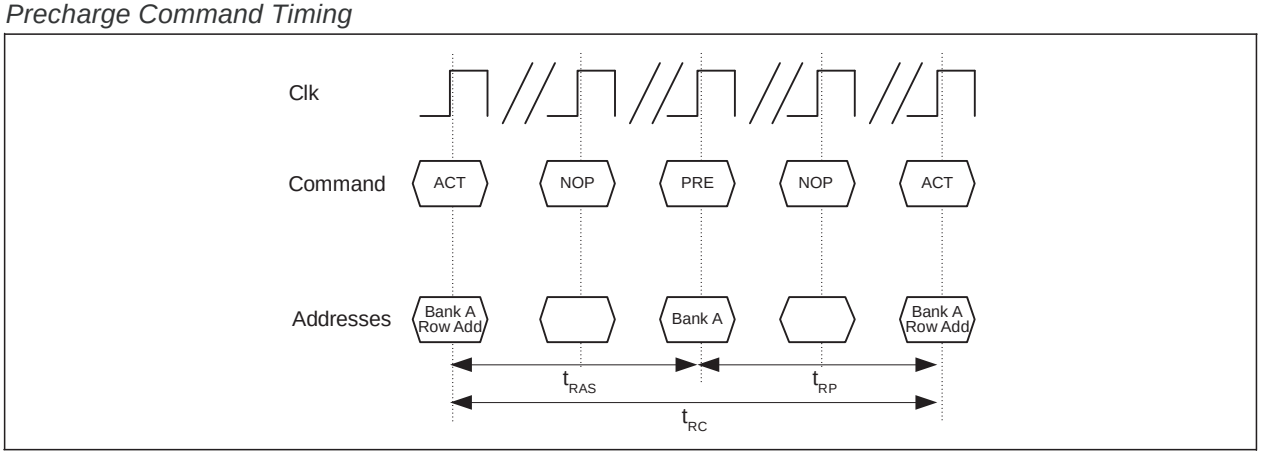
Precharge Command

This command is used to precharge or close a bank that has been activated. Precharge is initiated by issuing a Precharge command at the rising edge of the clock. The Precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank addresses BA0 and BA1 select the bank to be precharged. After a Precharge command, the analog delay t_{RP} has to be met until a new Activate command can be initiated to the same bank.

Table
Precharge Control

A10/ AP	BA1	BA0	Precharged
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

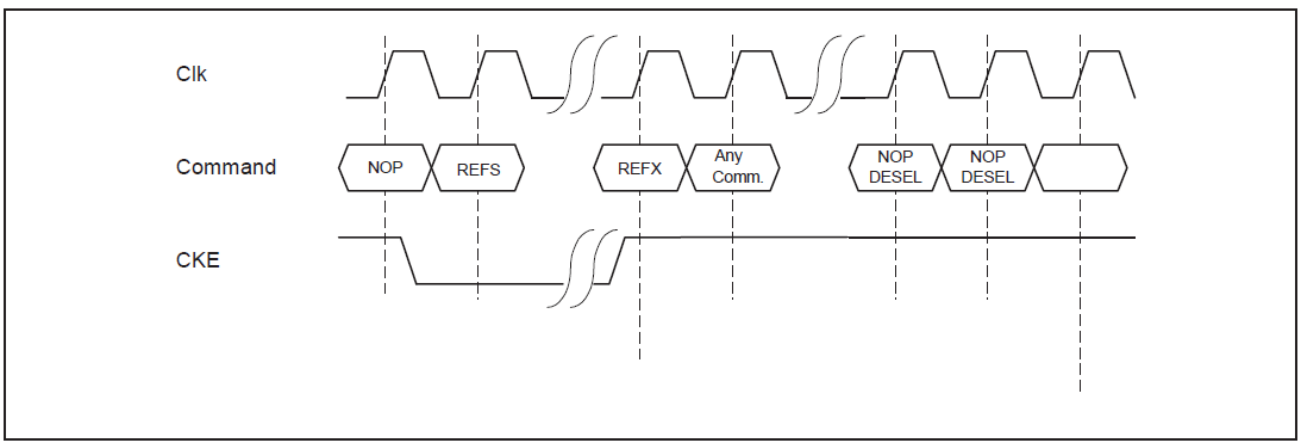
Precharge Command Timing



Self Refresh

The Self Refresh mode can be used to retain the data in the mobile DDR if the chip is powered down. To set the mobile DDR into a Self Refreshing mode, a Self Refresh command must be issued and CKE held low at the rising edge of the clock. Once the Self Refresh command is initiated, CKE must stay low to keep the device in Self Refresh mode. During the Self Refresh mode, all of the external control signals are disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. An internal timing generator guarantees the self refreshing of the memory content.

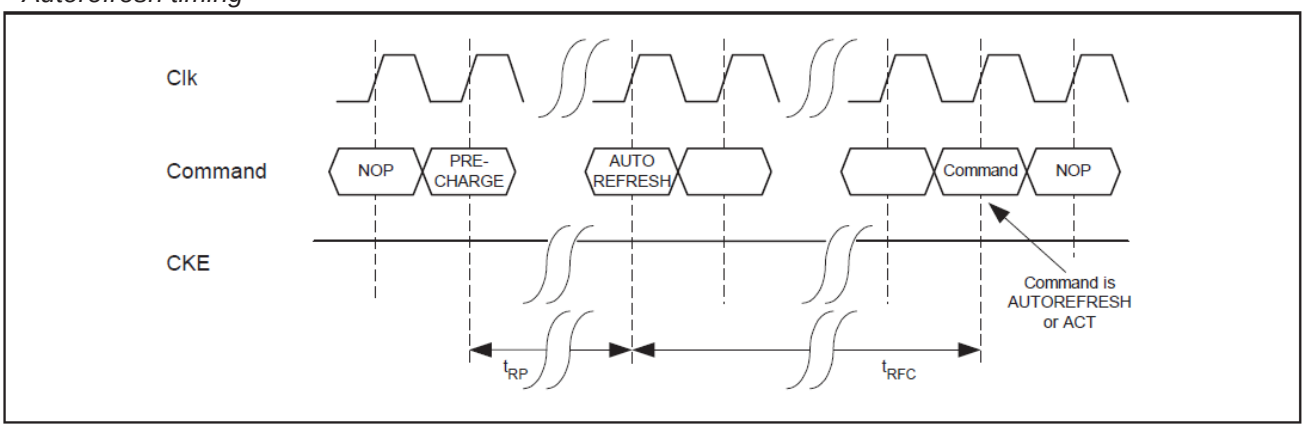
Self Refresh timing



Auto Refresh

The auto refresh function is initiated by issuing an Auto Refresh command at the rising edge of the clock. All banks must be precharged and idle before the Auto Refresh command is applied. No control of the external address pins is required once this cycle has started. All necessary addresses are generated in the device itself. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the t_{RFC}(min).

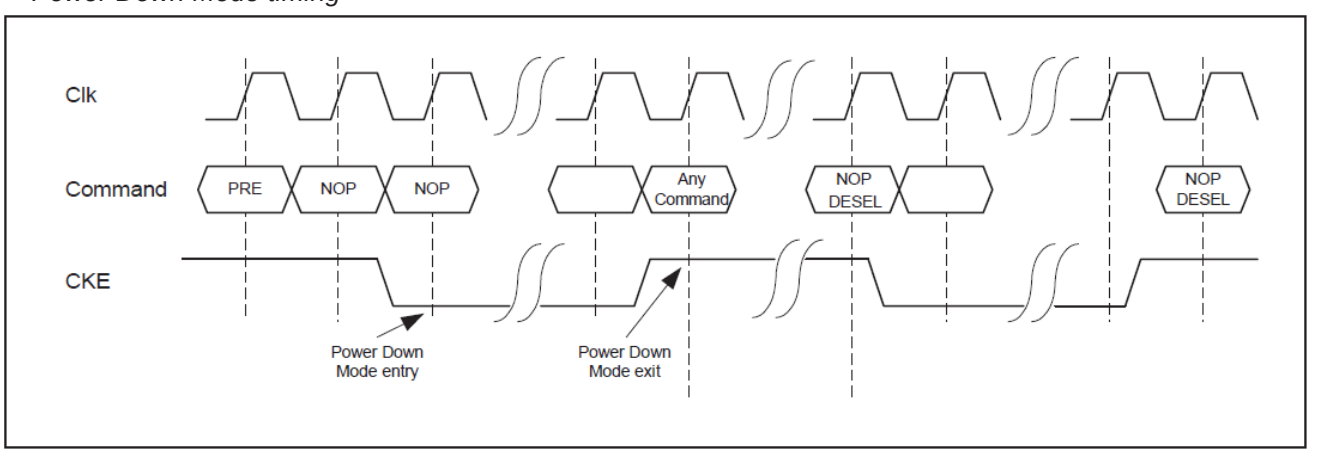
Autorefresh timing



Power Down Mode

The Power Down Mode is entered when CKE is set low and exited when CKE is set high. The CKE signal is sampled at the rising edge of the clock. Once the Power Down Mode is initiated, all of the receiver circuits except CLK and the CKE circuits are gated off to reduce power consumption. All banks can be set to idle state or stay activate during Power Down Mode, but burst activity may not be performed. After exiting from Power Down Mode, at least one clock cycle of command delay must be inserted before starting a new command. During Power Down Mode, refresh operations cannot be performed; therefore, the device cannot remain in Power Down Mode longer than the refresh period (t_{REF}) of the device.

Power Down Mode timing



Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to the memory (write cycle) or from the memory (read cycle). The burst length is programmable and set by address bits A0 - A3 during the Mode Register Setup command. The burst length controls the number of words that will be output after a read command or the number of words to be input after a write command. One word is 32 bits wide. The sequential burst length can be set to 2, 4 or 8 data words.

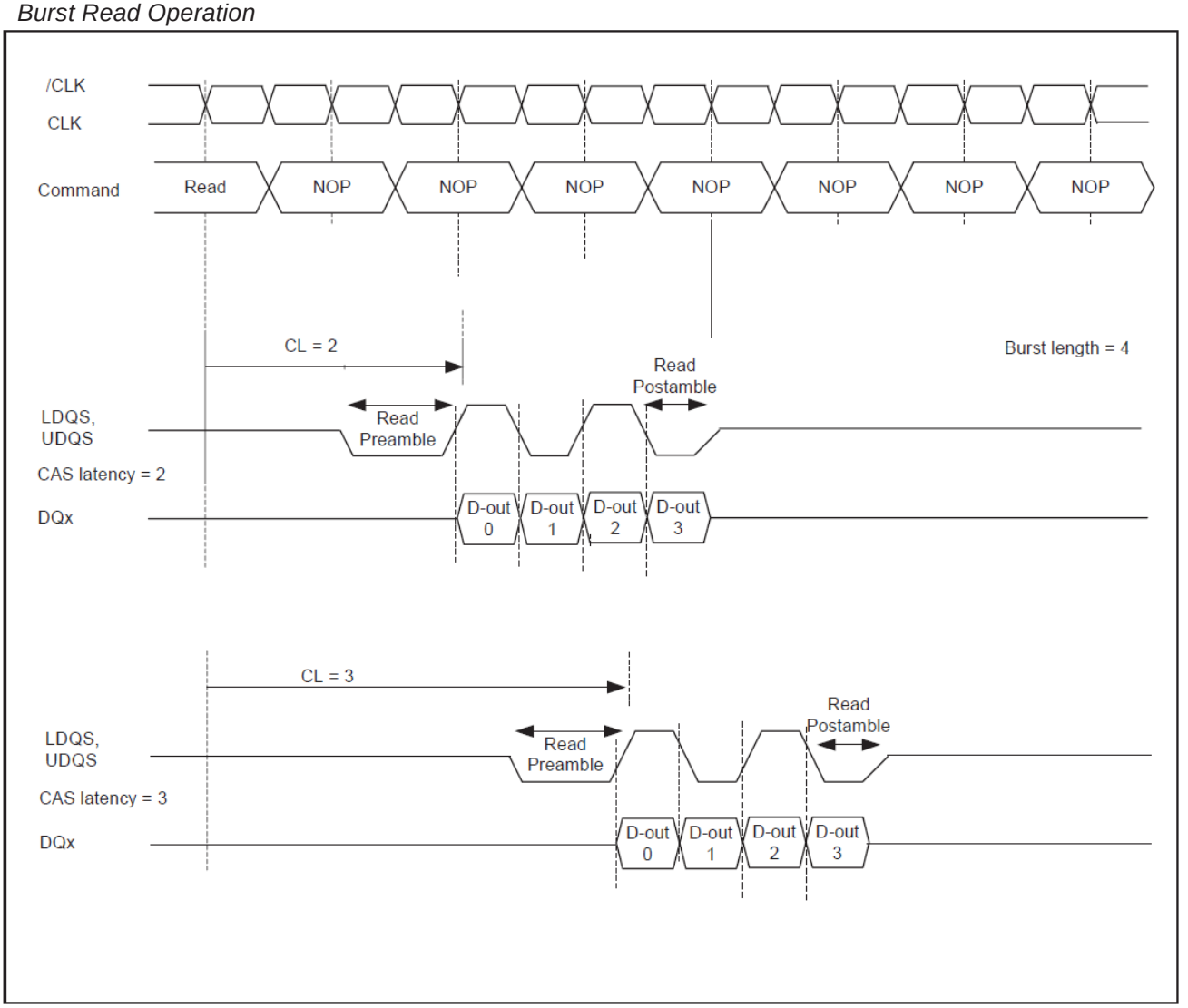
Burst Mode and Sequence

Burst Length	Starting Column Address				Order of Access within a Burst	
	A3	A2	A1	A0	Type = Sequential	Type = Interleaved
2				0	0 - 1	0 - 1
				1	1 - 0	1 - 0
4			0	0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
			0	1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
			1	0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
			1	1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8		0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
		0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
		0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
		0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
		1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
		1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
		1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
		1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0

Burst Read Operation: (READ)

The Burst Read operation is initiated by issuing a READ command at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs (A8.. A0) determine the starting address for the burst. The burst length (2, 4 or 8) must be defined in the Mode Register. The first data after the READ command is available depending on the CAS latency. The subsequent data is clocked out on the rising and falling edge of LDQS, UDQS until the burst is completed. The LDQS, UDQS signals are generated by the mobile DDR during the Burst Read Operation.

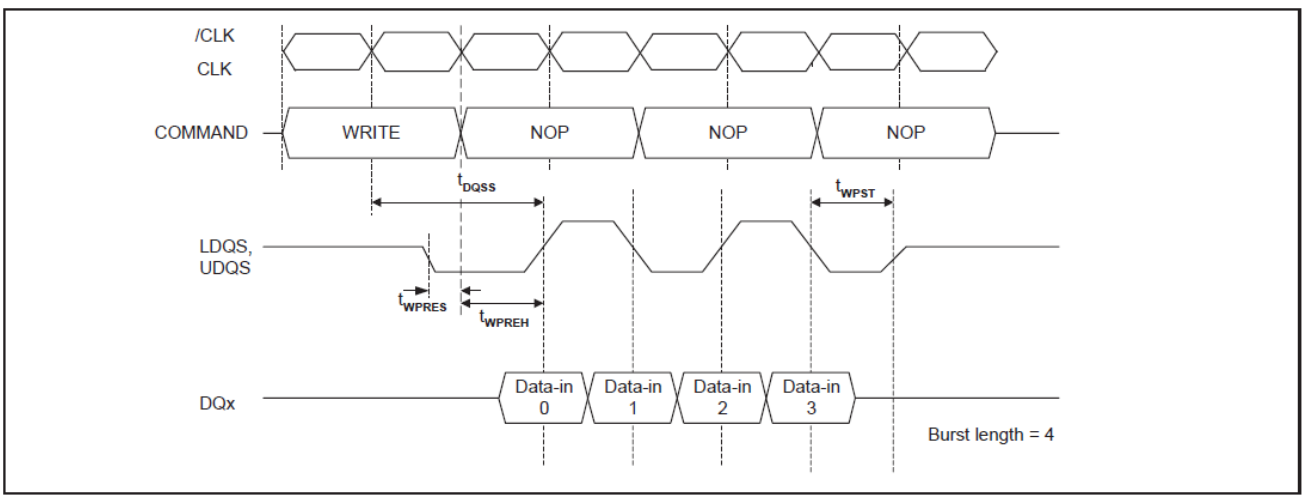
Burst Read Operation



Burst Write Operation (WRITE)

The Burst Write is initiated by issuing a WRITE command at the rising edge of the clock. The address inputs (A8 .. A0) determine starting column address. Data for the first burst write cycle must be applied on the DQ pins on the first rise edge of LDQS, UDQS follow WRITE command. The time between the WRITE command and the first corresponding edge of the data strobe is t_{DQSS}. The remaining data inputs must be supplied on each subsequent rising and falling edge of the data strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

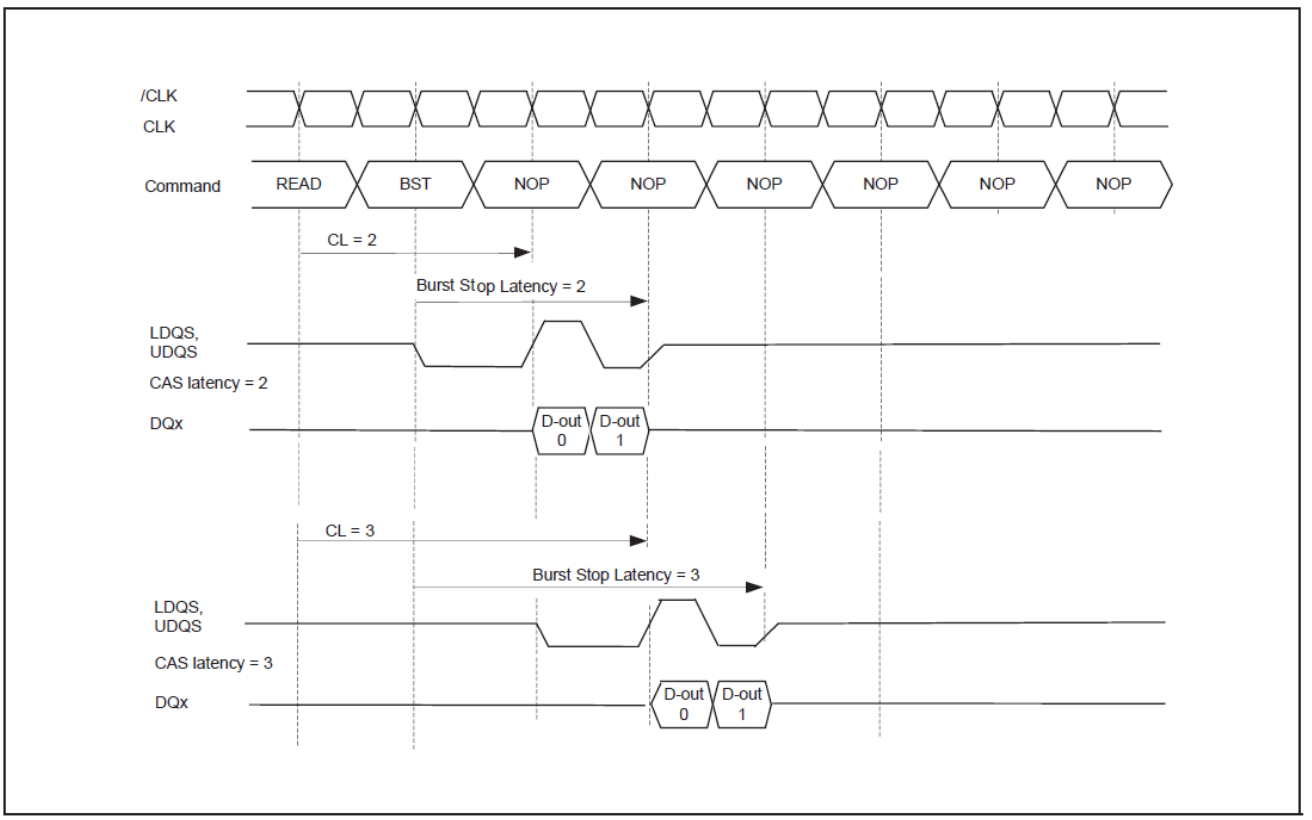
Burst Write Operation



Burst Stop Command (BST)

A Burst Stop is initiated by issuing a BURST STOP command at the rising edge of the clock. The Burst Stop Command has the fewest restrictions, making it the easiest method to terminate a burst operation before it has been completed. When the Burst Stop Command is issued during a burst read cycle, read data and LDQS, UDQS go to a high-Z state after a delay which is equal to the CAS latency set in the Mode Register. The Burst Stop latency is equal to the CAS latency CL. The Burst Stop command is not supported during a write burst operation. Burst Stop is also illegal during Read with Auto-Precharge.

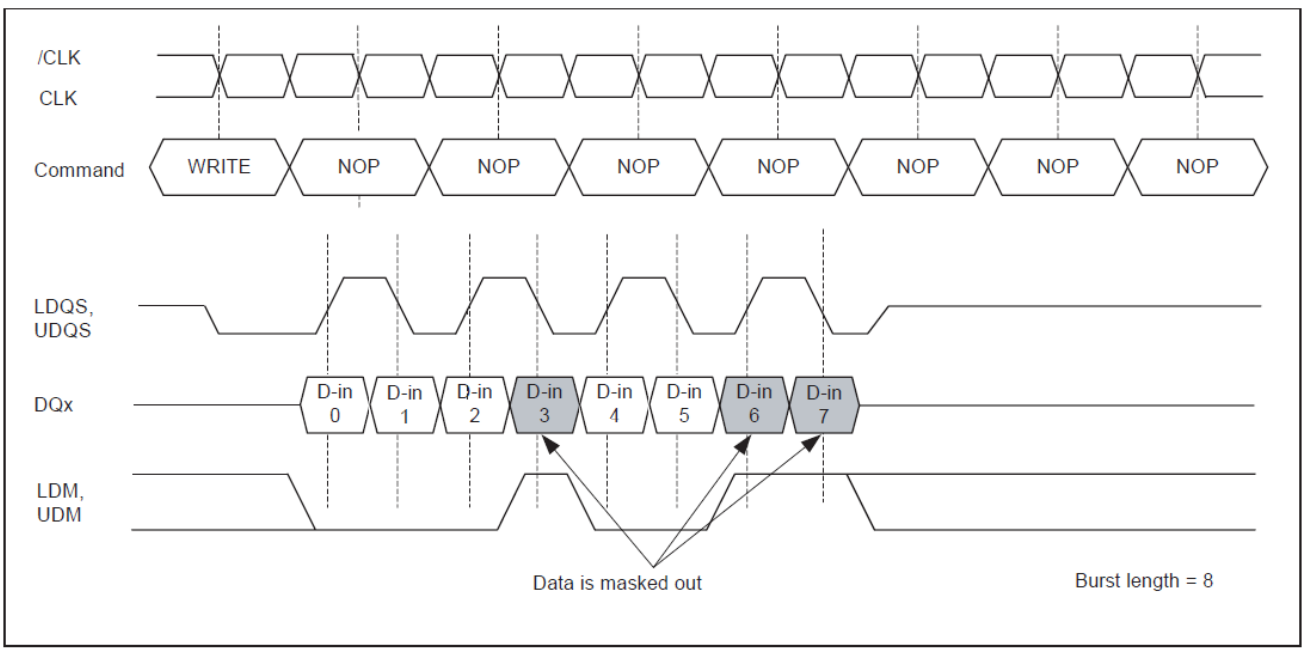
Burst Stop for Read



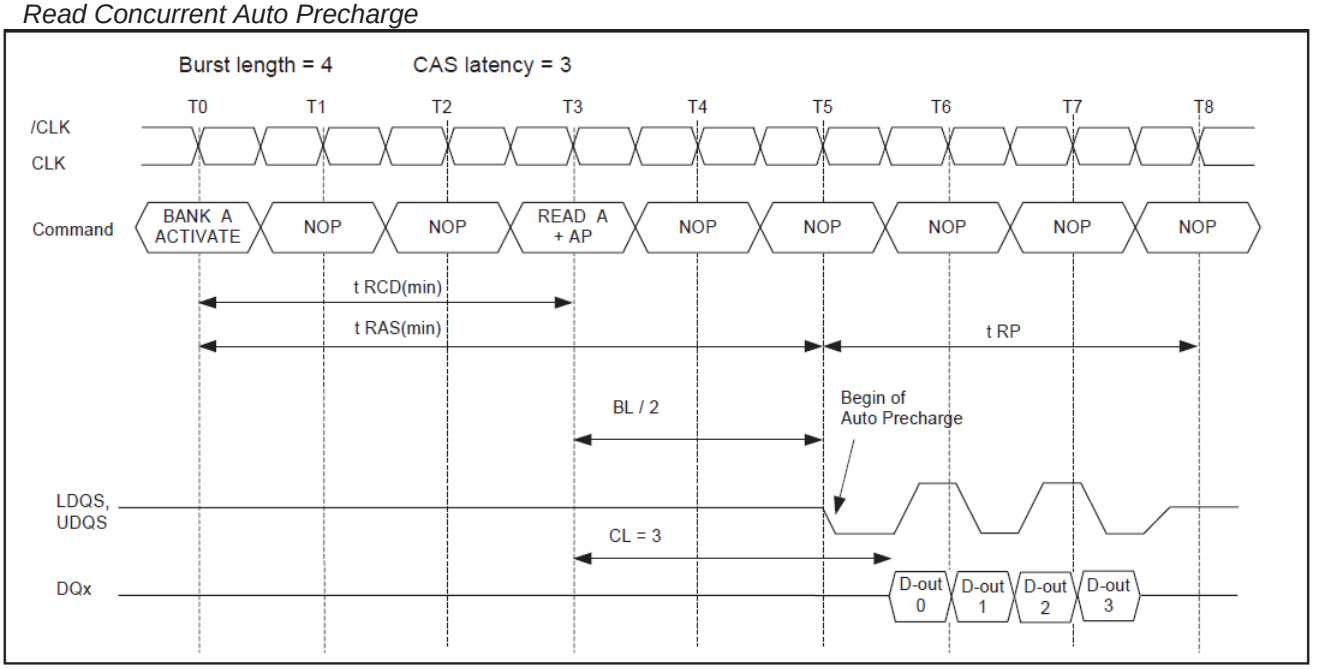
Data Mask (LDM, UDM) Function

The mobile DDR has a Data Mask function that can be used only during write cycles. When the Data Mask is activated, active high during burst write, the write operation is masked immediately. The LDM, UDM to data-mask latency zero. LDM and UDM can be issued at the rising or negative edge of Data Strobe.

Data Mask Timing



Read Concurrent Auto Precharge



Concurrent Read Auto Precharge Support

Asserted Command	For same Bank			For different Bank		
	T4	T5	T6	T4	T5	T6
READ	NO	NO	NO	NO	YES	YES
READ+AP	YES	YES	NO	NO	YES	YES
ACTIVATE	NO	NO	NO	YES	YES	YES
PRECHARGE	YES	YES	NO	YES	YES	YES

Note: This table is for the case of Burst Length = 4, CAS Latency =3 and t_{WR}=2 clocks

When READ with Auto Precharge is asserted, new commands can be asserted at T4,T5 and T6 as shown in Table

An Interrupt of a running READ burst with Auto Precharge i.e. at T4 and T5 to the same bank with another READ+AP command is allowed, it will extend the begin of the internal Precharge operation to the last READ+AP command.

Interrupts of a running READ burst with Auto Precharge i.e. at T4 are not allowed when doing concurrent command to another active bank. ACTIVATE or PRECHARGE commands to another bank are always possible while a READ with Auto Precharge operation is in progress.

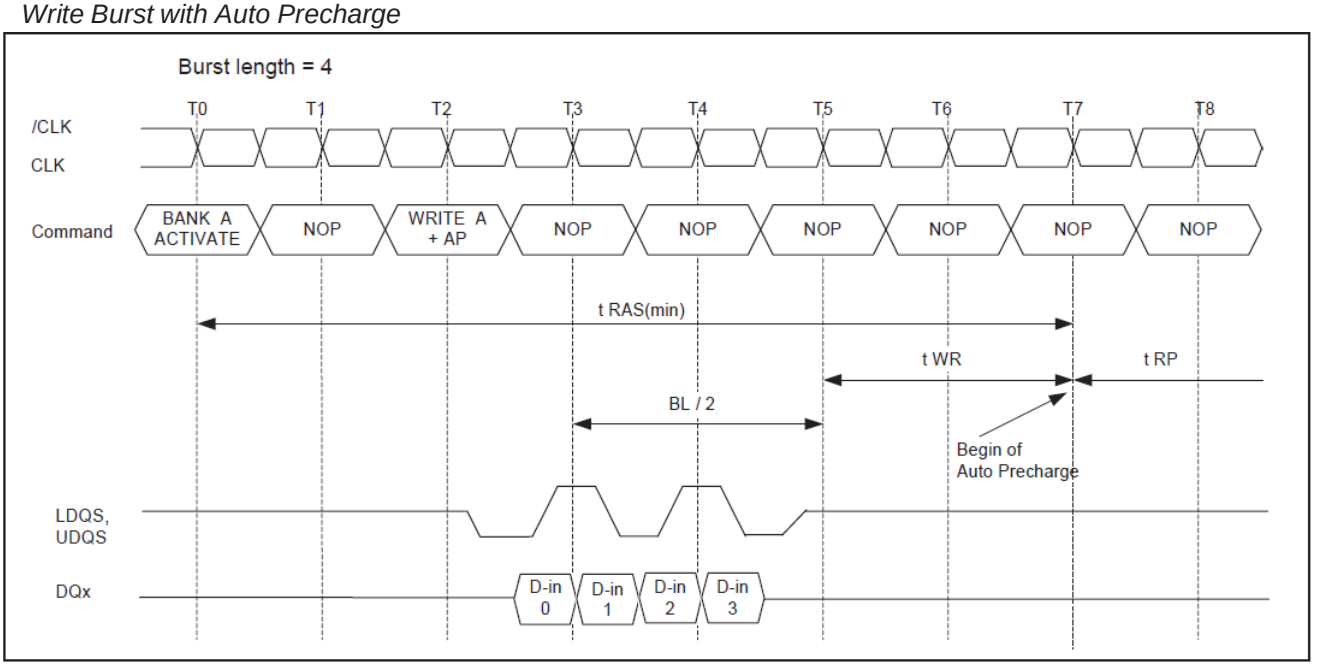
Write with Autoprecharge (WRITEA)

If A8 is high when a Write command is issued, the Write with Auto-Precharge function is performed. The internal precharge begins after the write recovery time t_{WR} and t_{RAS}(min) are satisfied.

If a Write with Auto Precharge command is initiated, the mobile DDR automatically enters the precharge operation at the first rising edge of CLK after the last valid edge of DQS (completion of the burst) plus the write recovery time t_{WR}. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the Precharge time (t_{RP}) has been satisfied.

If t_{RAS}(min) has not been satisfied yet, an internal interlock will delay the precharge operation until it is satisfied.

Write Burst with Auto Precharge



Note: t_{WR} starts at the first rising edge of clock after the last valid edge of the 4 DQSx.

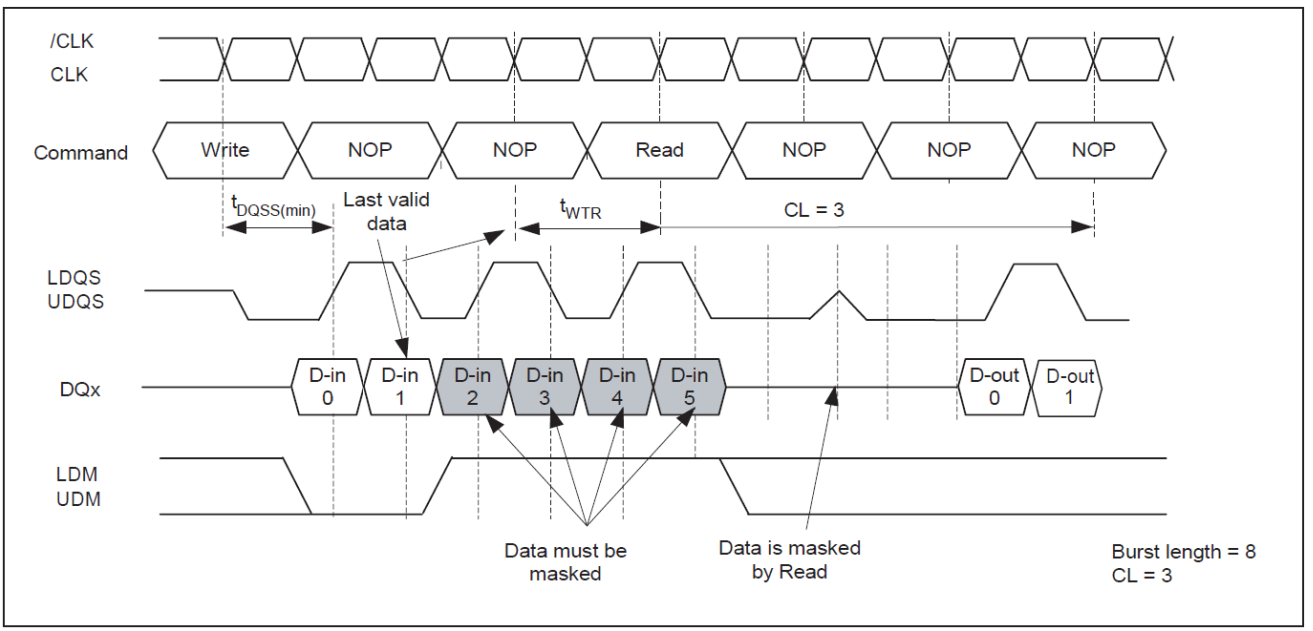
Concurrent Write Auto Precharge Support

Asserted Command	For same Bank						For different Bank				
	T3	T4	T5	T6	T7	T8	T3	T4	T5	T6	T7
WRITE	NO	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
WRITE+AP	YES	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
READ	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES
READ+AP	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES
ACTIVATE	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES
PRECHARGE	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES

When Write with Auto Precharge is asserted, new commands can be asserted at T3.. T8 as shown in Table.

An Interrupt of a running WRITE burst with Auto Precharge i.e. at T3 to the same bank with another WRITE+AP command is allowed as long as the burst is running, it will extend the begin of the internal Precharge operation to the last WRITE+AP command.
Interrupts of a running WRITE burst with Auto Precharge i.e. at T3 are not allowed when doing concurrent WRITE s to another active bank. Consecutive WRITE or WRITE+AP bursts (T4.. T7) to other open banks are possible. ACTIVATE or PRECHARGE commands to another bank are always possible while a WRITE with Auto Precharge operation is in progress.

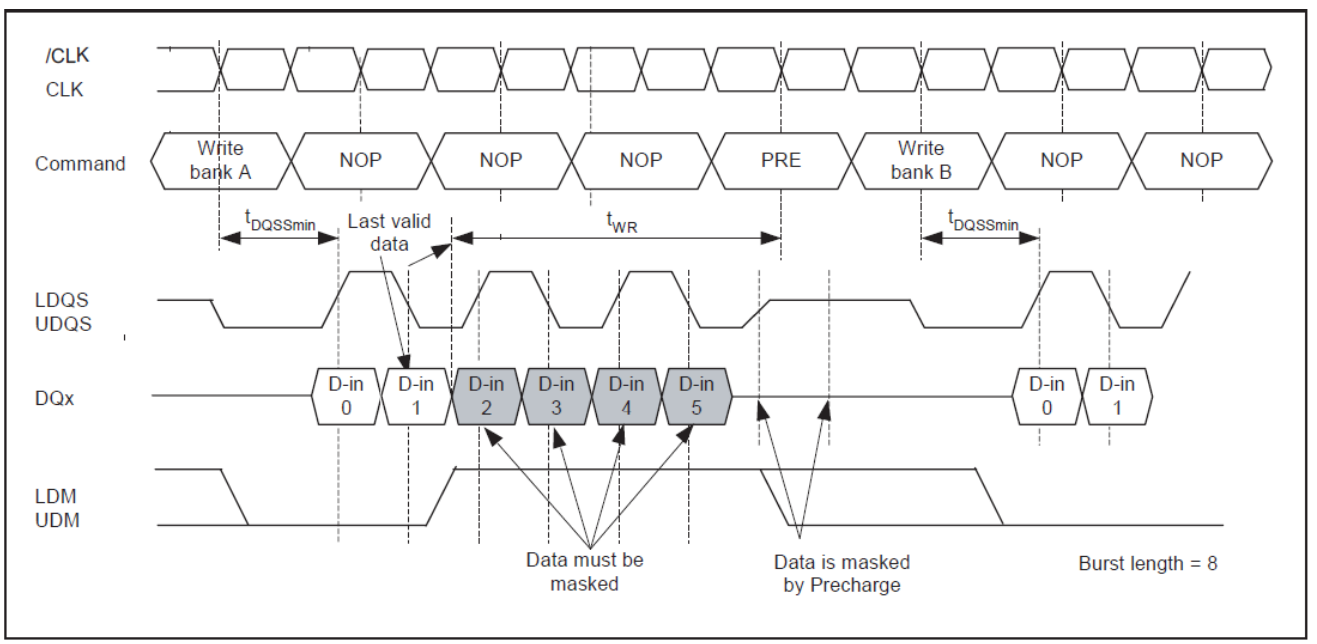
Write interrupted by Read



Write Interrupted by a Precharge

A Burst Write operation can be interrupted before completion of the burst by a Precharge of the same bank. Random column access is allowed. A Write Recovery time (t_{WR}) is required from the last data to Precharge command. When Precharge command is asserted, any residual data from the burst write cycle must be masked by LDM, UDM.

Write interrupted by Precharge



Command Table

Table Command Overview

Operation	Code	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	BA0	BA1	A10	A0-9 A11,12
Device Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X	X
Mode Register Setup	MRS	H	X	L	L	L	L	0	0	OPCODE	
Extended Mode Register Setup	EMRS	H	X	L	L	L	L	0	1	OPCODE	
Bank Activate	ACT	H	X	L	L	H	H	BA	BA	Row Address	
Read	READ	H	X	L	H	L	H	BA	BA	L	Col.
Read with Auto Precharge	READA	H	X	L	H	L	H	BA	BA	H	Col.
Write Command	WRITE	H	X	L	H	L	L	BA	BA	L	Col.
Write Command with Auto Precharge	WRITEA	H	X	L	H	L	L	BA	BA	H	Col.
Burst Stop	BST	H	X	L	H	H	L	X	X	X	X
Precharge Single Bank	PRE	H	X	L	L	H	L	BA	BA	L	X
Precharge All Banks	PREAL	H	X	L	L	H	L	X	X	H	X
Autorefresh	REF	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	REFX	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	SREFEX	L L	H H	H L	X H	X H	X H	X X	X X	X X	X X
Power Down Mode Entry *(Note 1)*	PWDNEN	H H	L L	H L	X H	X H	X H	X X	X X	X X	X X
Power Down Mode Exit	PWDNEX	L	H	H L	X valid	X valid	X valid	X	X	X	X

Note: 1: The Power Down Mode Entry command is illegal during Burst Read or Burst Write operations.

Function Truth Table I

Current State	Command	Address	Action	Notes
IDLE	DESEL	X	NOP	3
	NOP	X	NOP	3
	BST	X	NOP	3
	READ / READA	BA,CA,A10	ILLEGAL	1
	WRITE / WRITEA	BA,CA,A10	ILLEGAL	1
	ACT	BA, RA	Bank Active	
	PRE / PREAL	BA, A10	NOP	
	AREF / SREF	X	AUTO-Refresh or Self-Refresh	4
	MRS / EMRS	Op-Code	Mode Register Set or Extended Mode Register Set	
ROW ACTIVE	DESEL	X	NOP	
	NOP	X	NOP	
	BST	X	NOP	
	READ / READA	BA, CA, A10	Begin Read, Determine Auto Precharge	9
	WRITE / WRITEA	BA, CA, A10	Begin Write, Determine Auto Precharge	9
	ACT	BA, RA	ILLEGAL	1, 5
	PRE / PREAL	BA, A10	Precharge / Precharge All	6
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
READ	DESEL	X	Continue burst to end	
	NOP	X	Continue burst to end	
	BST	X	Terminate Burst	
	READ / READA	BA, CA, A10	Terminate burst, Begin New Read, Determine Auto-Prechgarge	7
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	2, 7
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA ,A10	Terminate Burst / Precharge	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	Op-Code	ILLEGAL	
READ with Auto Precharge	DESEL	X	Continue burst to end, Precharge	
	NOP	X	Continue burst to end, Precharge	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA ,A10	ILLEGAL	1
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	Op-Code	ILLEGAL	

Current State	Command	Address	Action	Notes
WRITE	DESEL	X	Continue burst to end	
	NOP	X	Continue burst to end	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A10	Terminate Burst, Begin Read, Determine Auto-Precharge.	7, 8
	WRITE / WRITEA	BA, CA, A10	Terminate Burst, Begin new Write, Determine Auto-Precharge	2, 7
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA, A10	Terminate Burst , Precharge	8
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
WRITE with Auto Precharge	DESEL	X	Continue burst to end, Precharge	
	NOP	X	Continue burst to end, Precharge	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA , A10	ILLEGAL	1
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
ROW ACTIVATING	DESEL	X	NOP (Row Active after t_{RCD})	
	NOP	X	NOP (Row Active after t_{RCD})	
	BST	X	NOP (Row Active after t_{RCD})	
	READ / READA	BA, CA, A10	ILLEGAL	1, 9
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	1, 9
	ACT	BA, RA	ILLEGAL	1, 5
	PRE / PREAL	BA, A10	ILLEGAL	1, 6
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
PRECHARGE	DESEL	X	NOP (Row Idle after t_{RP})	
	NOP	X	NOP (Row Idle after t_{RP})	
	BST	X	NOP (Row Idle after t_{RP})	
	READ / READA	BA, CA, A10	ILLEGAL	1
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	1
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA, A10	NOP (Row Idle after t_{RP}) 1	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

Current State	Command	Address	Action	Notes
WRITE RECOVERING	DESEL	X	NOP (Row Active after t_{WR})	
	NOP	X	NOP (Row Active after t_{WR})	
	BST	X	NOP (Row Active after t_{WR})	
	READ / READA	BA, CA, A10	Begin Read, Determine Auto-Precharge	2
	WRITE / WRITEA	BA, CA, A10	Begin Write, Determine Auto-Precharge	
	ACT	BA, RA	ILLEGAL	2
	PRE / PREAL	BA ,A10	ILLEGAL	1, 10
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
WRITE RECOVERING with AUTO-PRECHARGE	DESEL	X	NOP (Precharge after t_{WR})	
	NOP	X	NOP (Precharge after t_{WR})	
	BST	X	NOP (Precharge after t_{WR})	
	READ / READA	BA, CA, A10	ILLEGAL	1, 2
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	1
	ACT	BA, RA	ILLEGAL	1
	PRE / PREAL	BA ,A10	ILLEGAL	1
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
REFRESH	DESEL	X	NOP (Idle after t_{RC})	
	NOP	X	NOP (Idle after t_{RC})	
	BST	X	NOP (Idle after t_{RC})	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	11
	PRE / PREAL	BA ,A10	ILLEGAL	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
(EXTENDED) MODE REGISTER SET	DESEL	X	NOP (Idle after two clocks)	
	NOP	X	NOP (Idle after two clocks)	
	BST	X	NOP (Idle after two clocks)	
	READ / READA	BA, CA, A10	ILLEGAL	
	WRITE / WRITEA	BA, CA, A10	ILLEGAL	
	ACT	BA, RA	ILLEGAL	
	PRE / PREAL	BA ,A10	ILLEGAL	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

Note: All entries assume the CKE was High during the preceding clock cycle
Note: 1. Illegal to bank specified states; function may be legal in the bank indicated by BAx, depending on the state of that bank
Note: 2. Must satisfy bus contention, bus turn around, write recovery requirements.
Note: 3. If both banks are idle, and CKE is inactive, the device will enter Power Down Mode. All input buffers except CKE, CLK and CLK# will be disabled.
Note: 4. If both banks are idle, and CKE is deactivated coincidentally with an AutoRefresh command, the device will enter SelfRefresh Mode. All input buffers except CKE will be disabled. Note: 5. Illegal, if tRRD is not satisfied.
Note: 6. Illegal, if tRAS is not satisfied.
Note: 7. Must satisfy burst interrupt condition.
Note: 8. Must mask two preceding data bits with the DM pin. Note: 9. Illegal, if tRCD is not satisfied.
Note: 10. Illegal, if tWR is not satisfied.
Note: 11. Illegal, if tRC is not satisfied.

Abbreviations:

H	High Level
L	Low Level
X	Don't Care
V	Valid Data Input
RA	Row Address
BA	Bank Address
PA	Precharge All
NOP	No Operation
CA	Column Address
Ax	Address Line x

FUNCTION TRUTH TABLE for CKE

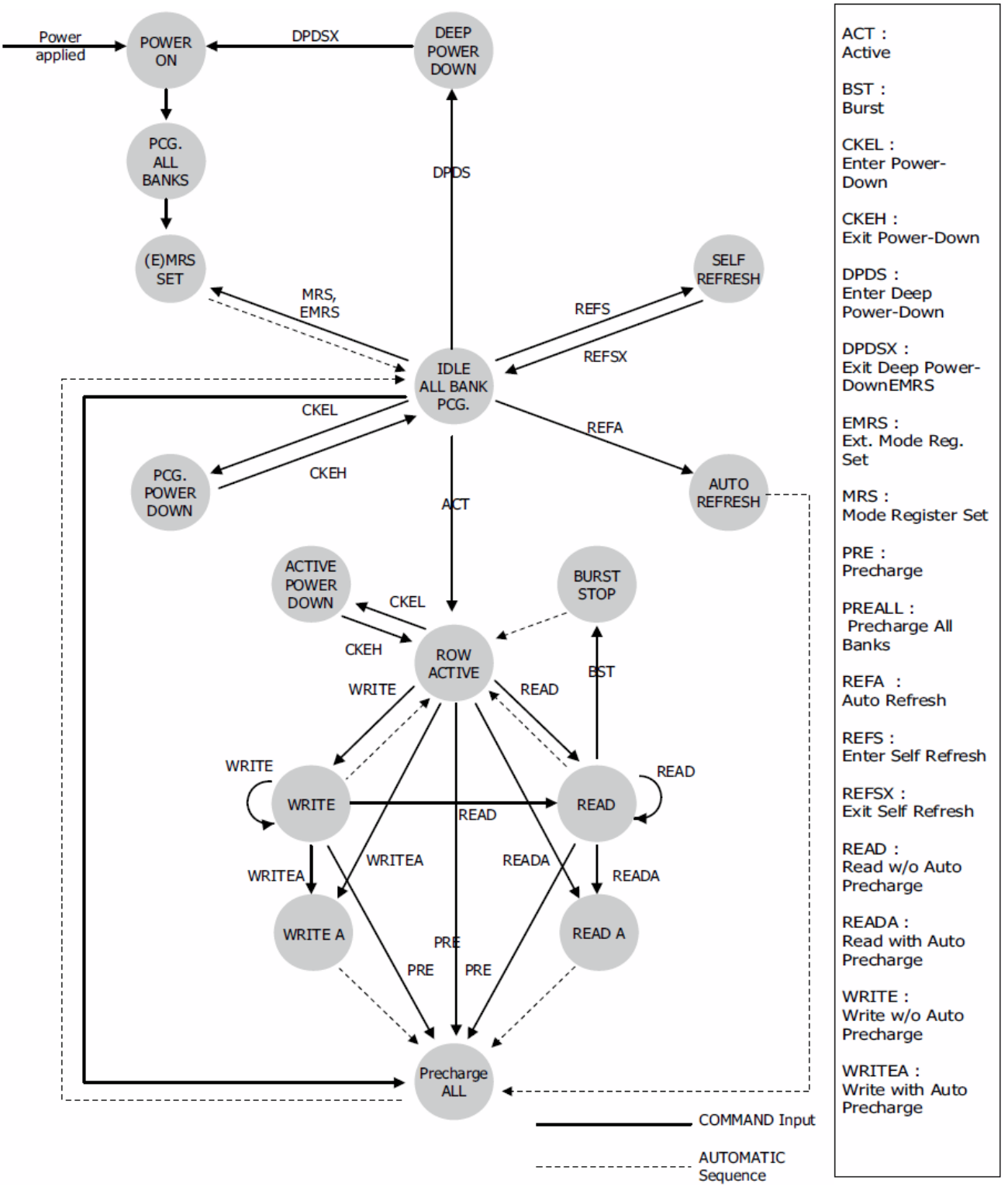
Current State	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	Address	Action	Notes
SELF REFRESH	H	L	L	L	L	H	X	Self Refresh Entry	1
	L	H	H	X	X	X	X	Exit Self-Refresh	1
	L	H	L	H	H	H	X	Exit Self-Refresh	1
	L	H	L	H	H	L	X	ILLEGAL	1
	L	H	L	H	H	X	X	ILLEGAL	1
	L	H	L	L	L	X	X	ILLEGAL	1
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	1
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down (Idle after t_{PDEX})	1
	L	L	X	X	X	X	X	NOP (Maintain Power Down)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2
	H	L	L	L	L	H	X	Enter Self Refresh	3
	H	L	H	X	X	X	X	Enter Power-Down	2
	H	L	L	H	H	H	X	Enter Power-Down	2
	H	L	L	H	H	L		ILLEGAL	2
	H	L	L	H	L	X		ILLEGAL	2
	H	L	L	L	X	X		ILLEGAL	2
	L	X	X	X	X	X	X	Refer to Power Down in this table	
All other states	H	H	X	X	X	X	X	Refer to Funtion Truth Table	

Note: 1. CKE low-to-high transition re-enables inputs asynchronously. A minimum setup time to CLK must be satisfied before any commands other than EXIT are executed.
Note: 2. Power Down can be entered when all banks are idle (banks can be active or precharged)
Note: 3. Self Refresh can be entered only from the Precharge / Idle state.

Abbreviations:

H	High Level
L	Low Level
X	Don't Care
V	Valid Data Input
RA	Row Address
BA	Bank Address
PA	Precharge All
NOP	No Operation
CA	Column Address

Mobile DDR SDRAM operation
State Diagram



IDD Max Specifications and Conditions

Parameter	Version				
	Symbol	-5	-6	-75	Unit
Operating Current: one bank; active/ precharge; $t_{RC} = t_{RCMIN}$; $t_{CK} = t_{CKMIN}$;DQ, DM, and DQS inputs changing once per clock cycle; address and control inputs changing once every two clock cycles. CS = high between valid commands.	IDD0	90	80	75	mA
Operating Current: one bank; active/read/precharge; Burst = 4; $\overline{CS}$ = high between valid commands.	IDD1	115	100	85	mA
Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE $\leq V_{ILMAX}$; $t_{CK} = t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM	IDD2P	12	12	12	mA
Precharge Floating Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle;CKE $\geq V_{IHMIN}$; $t_{CK} = t_{CKMIN}$, address and other control inputs changing once per clock cycle, $V_{IN} = V_{REF}$ for DQ, DQS and DM.	IDD2F	35	30	25	mA
Precharge Quiet Standby Current: $\overline{CS} \geq V_{IHMIN}$, all banks idle; CKE $\geq V_{IHMIN}$; $t_{CK} = t_{CKMIN}$, address and other control inputs stable at $\geq V_{IHMIN}$ or $\leq V_{ILMAX}$; $V_{IN}=V_{REF}$ for DQ, DQS and DM.	DD2Q	35	25	25	mA
Active Power-Down Standby Current: one bank active; power-down mode; CKE $\leq V_{ILMAX}$; $t_{CK}= t_{CKMIN}$; $V_{IN} = V_{REF}$ for DQ, DQS and DM.	IDD3P	40	35	35	mA
Active Standby Current: one bank active; $\overline{CS} \geq V_{IHMIN}$; CKE $\geq V_{IHMIN}$; $t_{RC} = t_{RASMAX}$; $t_{CK} = t_{CKMIN}$; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD3N	65	60	55	mA
Operating Current: one bank active; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} = t_{CKMIN}$; I_{OUT} = 0 mA	IDD4R	180	150	130	mA
Operating Current: one bank active; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; 50% of data outputs changing on every clock edge; CL = 2 for DDR200 and DDR266A, CL = 3 for DDR333; $t_{CK} =$	IDD4W	165	135	120	mA
Auto-Refresh Current: $t_{RC} = t_{RFCMIN}$, burst refresh	IDD5	190	175	165	mA
Self-Refresh Current: CKE $\leq$ 0.2 V; external clock on; $t_{CK} = t_{CKMIN}$	IDD6	14	14	14	mA
Operating Current: four bank; four bank interleaving with BL = 4	IDD7	255	215	185	mA

Partial Array Self Refresh Current (PASR)

Parameter & Test Condition	Extended Mode Register A[2:0] Tcase [°C]	Symb.	max.	Unit	Note
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, full array activations, all banks	85°C max.	ICC6	-	mA	-
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, 1/2 array activations	85°C max.	ICC6	-	mA	-
Self Refresh Current Self Refresh Mode CKE = 0.2V, tck = infinity, 1/4 array activation	85°C max.	ICC6	-	mA	-

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.7	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-0.5 ~ 2.7	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

Note:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Capacitance (V_{DD} = 1.8V, T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Input capacitance, CK, CK	CCK	1.5	3.0	pF	-
Input capacitance delta, CK, CK	CDCK	-	0.25	pF	-
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	-
Input capacitance delta, all other input-only pins	CDI	-	0.5	pF	-
Input/output capacitance, DQ, DM, DQS	CIO	3.0	5.0	pF	1
Input/output capacitance delta, DQ, DM, DQS	CDIO	-	0.5	pF	1

Note:

1. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

Power & DC Operating Conditions (LVCMOS In/Out)

Recommended operating conditions (Voltage referenced to V_{SS} = 0V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage	VDD	1.7	1.9	V	-
I/O Supply Voltage	VDDQ	1.7	1.9	V	-
Address and Command Inputs (A0 - An, BA0, BA1, CKE, CS, RAS, CAS, WE)					
Input High Voltage	VIH	0.8 * VDDQ	VDDQ +0.3	V	-
Input Low Voltage	VIL	-0.3	0.2 * VDDQ	V	-
Clock Inputs (CK, CK)					
DC Input Voltage	VIN	-0.3	VDDQ +0.3	V	-
DC Input Differential Voltage	VID(DC)	0.4 * VDDQ	VDDQ +0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6 * VDDQ	VDDQ +0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4 * VDDQ	0.6 * VDDQ	V	3
Data Inputs (DQ, DM, DQS)					
DC Input High Voltage	VIHD(DC)	0.7 * VDDQ	VDDQ +0.3	V	-
DC Input Low Voltage	VILD(DC)	-0.3	0.3 * VDDQ	V	-
AC Input High Voltage	VIHD(AC)	0.8 * VDDQ	VDDQ +0.3	V	-
AC Input Low Voltage	VILD(AC)	-0.3	0.2 * VDDQ	V	-
Data Outputs (DQ, DQS)					
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9 * VDDQ	-	V	-
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1 * VDDQ	V	-

NOTES:

1. All voltages referenced to VSS and VSSQ must be same potential.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5 * VDDQ and must track variations in the DC level of the same.

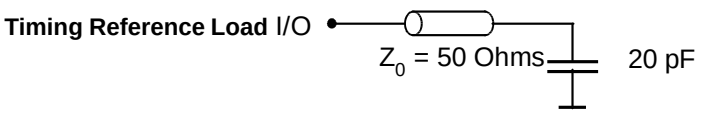
AC Timing Parameters & Specification

PARAMETER		SYMBOL	LPDDR266		LPDDR333		LPDDR400		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
DQ output access time from CK/$\overline{CK}$		tAC	2.0	6.5	2.0	5.5	2.0	5.0	ns	-
DQS output access time from CK/$\overline{CK}$		tDQSCK	2.0	6.5	2.0	5.5	2.0	5.0	ns	-
Clock high-level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	-
Clock low-level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	-
Clock half period		tHP	min (tCL, tCH)	-	min (tCL, tCH)	-	min (tCL, tCH)	-	ns	10, 11
Clock cycle time	CL = 4	tCK	-	-	-	100	5.0	100	ns	12
	CL = 3		7.5		6.0		5.0			
	CL = 2		12		12		12			
DQ and DM input setup time	fast slew rate	tDS	0.8	-	0.6	-	0.48	-	ns	13,14,15
	slow slew rate		0.9	-	0.7	-	0.58	-	ns	13,14,16
DQ and DM input hold time	fast slew rate	tDH	0.8	-	0.6	-	0.48	-	ns	13,14,15
	slow slew rate		0.9	-	0.7	-	0.58	-	ns	13,14,16
DQ and DM input pulse width		tDIPW	1.8	-	2.1	-	1.8	-	ns	17
Address and control input setup time	fast slew rate	tIS	1.3	-	1.1	-	0.9	-	ns	15,18
	slow slew rate		1.5	-	1.3	-	1.1	-	ns	16,18
Address and control input hold time	fast slew rate	tIH	1.3	-	1.1	-	0.9	-	ns	15,18
	slow slew rate		1.5	-	1.3	-	1.1	-	ns	16,18
Address and control input pulse width		tIPW	3.0	-	2.7	-	2.3	-	ns	17
DQ & DQS low-impedance time from CK/$\overline{CK}$		tLZ	1.0	-	1.0	-	1.0	-	ns	19
DQ & DQS high-impedance time from CK/$\overline{CK}$		tHZ	-	6.5	-	5.5	-	5.0	ns	19
DQS - DQ skew		tDQSQ	-	0.6	-	0.5	-	0.4	ns	20
DQ / DQS output hold time from DQS		tQH	tHP-tQHS	-	tHP-tQHS	-	tHP-tQHS		ns	11
Data hold skew factor		tQHS		0.75		0.65		0.5	ns	1-1
Write command to 1st DQS latching transition		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	-
DQS input high-level width		tDQSH	0.4	-	0.4	-	0.4	-	tCK	-
DQS input low-level width		tDQSL	0.4	-	0.4	-	0.4	-	tCK	-
DQS falling edge to CK setup time		tDSS	0.2	-	0.2	-	0.2	-	tCK	-
DQS falling edge hold time from CK		tDSH	0.2	-	0.2	-	0.2	-	tCK	-
MODE REGISTER SET command period		tMRD	2	-	2	-	2	-	tCK	-

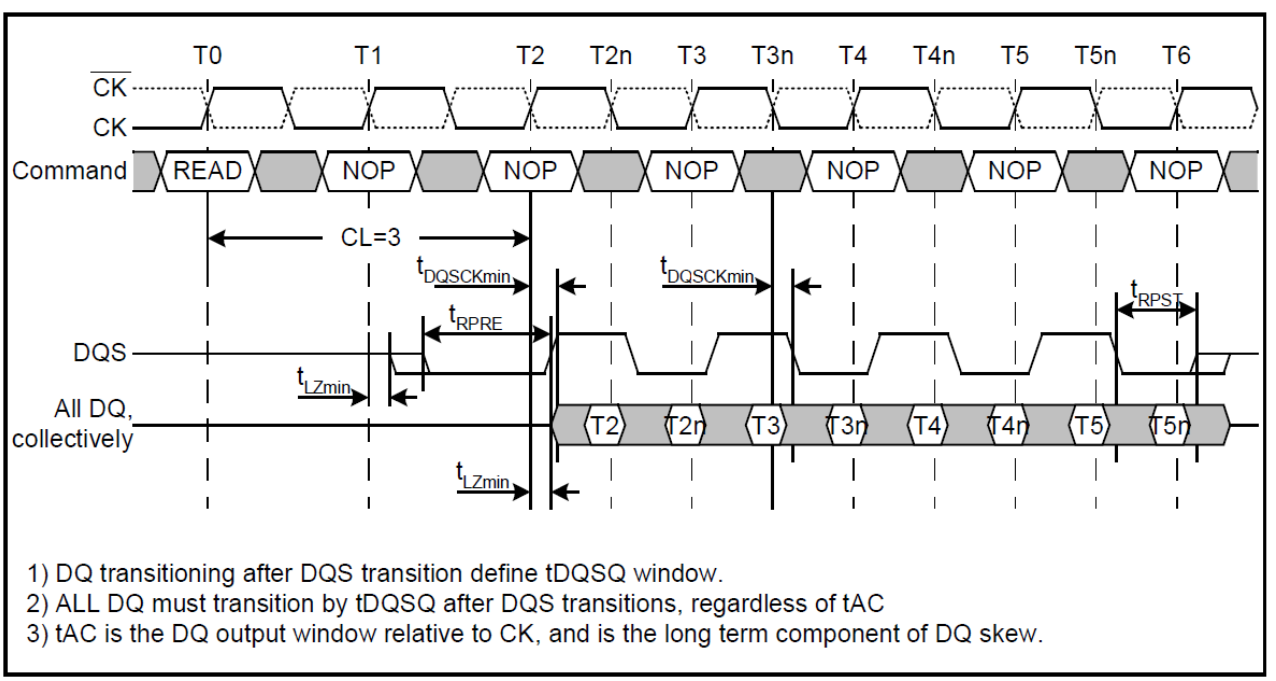
PARAMETER		SYMBOL	LPDDR266		LPDDR333		LPDDR400		UNIT	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
Write preamble setup time		tWPRES	0	-	0	-	0	-	ns	21
Write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	22
Write preamble		tWPRE	0.25	-	0.25	-	0.25	-	tCK	-
Read preamble	CL = 2	tRPRE	0.5	1.1	0.5	1.1	0.5	1.1	tCK	23
	CL = 3		0.9	1.1	0.9	1.1	0.9	1.1		
	CL = 4		-	-	-	-	0.9	1.1		
Read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	-
ACTIVE to PRECHARGE command period		tRAS	45	70,000	42	70,000	40	70,000	ns	-
ACTIVE to ACTIVE command period		tRC	tRAS+ tRP	-	tRAS+ tRP	-	tRAS+ tRP	-	ns	-
AUTO REFRESH to ACTIVE / AUTO REFRESH command period		tRFC	140	-	140	-	140	-	ns	-
ACTIVE to READ or WRITE delay		tRCD	22.5	-	18	-	15	-	ns	24
			30	-	30		20		ns	25
PRECHARGE command period		tRP	22.5	-	18	-	15	-	ns	24
			30	-	30		20		ns	25
ACTIVE bank A to ACTIVE bank B delay		tRRD	15	-	12	-	10	-	ns	-
WRITE recovery time		tWR	15	-	15	-	15	-	ns	-
Auto precharge write recovery + precharge time		tDAL	-	-	-	-	-	-	tCK	26
Internal write to Read command delay		tWTR	1	-	2	-	2	-	tCK	-
Self refresh exit to next valid command delay		tXSR	200	-	200	-	200	-	ns	27
Exit power down to next valid command delay		tXP	25	-	25	-	25	-	ns	28
CKE min. pulse width (high and low pulse width)		tCKE	2	-	2	-	2	-	tCK	-
Refresh Period		tREF	64	64	64	64	64	64	ms	-
Average periodic refresh interval		tREFI	7.8	7.8	7.8	7.8	7.8	7.8	µs	29, 30
MRS for SRR to READ		tSRR	2	-	2	-	2	-	tCK	-
READ of SRR to next valid command		tSRC	CL +1	-	CL +1	-	CL +1	-	tCK	-

NOTES:

1. All voltages referenced to *VSS*.
2. All parameters assume proper device initialization.
3. Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10 pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.



5. The CK/$\overline{CK}$ input reference voltage level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference voltage level for signals other than CK/$\overline{CK}$ is *VDDQ*/2.
6. The timing reference voltage level is *VDDQ*/2.
7. AC and DC input and output voltage levels are defined in the section for Electrical Characteristics and AC/DC operating conditions.
8. A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for all parameters.
9. CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (see figure); with CL = 2 the first data element is valid at (tCK + tAC) after the clock at which the READ command was registered; with CL = 4 the first data element is valid at (3 * tCK + tAC) after the clock at which the READ command was registered.

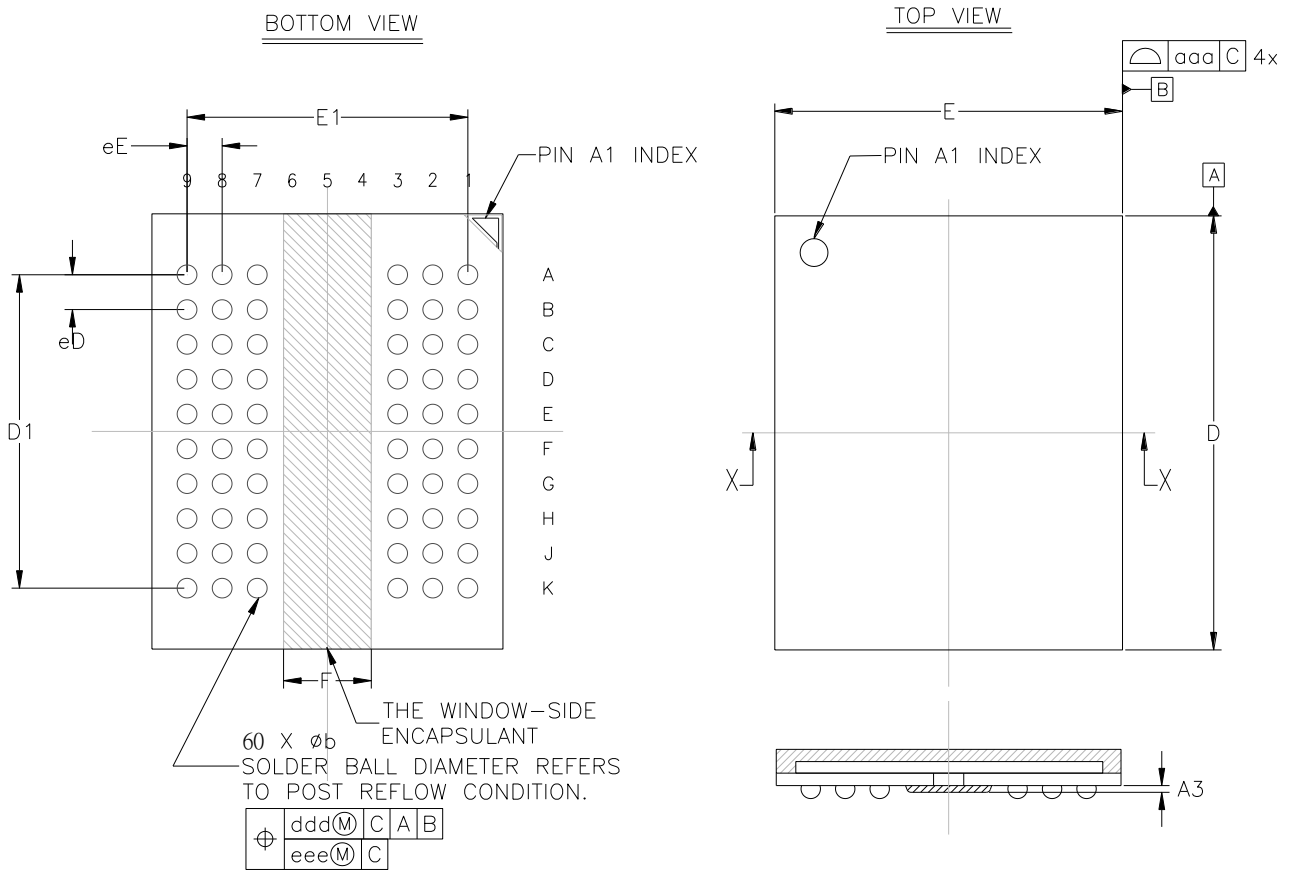


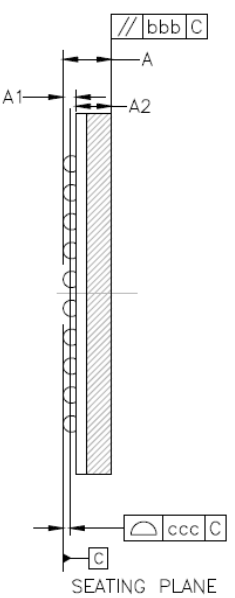
10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)

11. tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCL, tCH). tQHS accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
12. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
13. The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.
14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
15. Input slew rate ≥ 1.0 V/ns.
16. Input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.
17. These parameters guarantee device timing but they are not necessarily tested on each device.
18. The transition time for address and command inputs is measured between V_{IH} and V_{IL}.
19. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving ($_{HZ}$), or begins driving ($_{LZ}$).
20. t_{DQSQ} consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
21. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before the corresponding CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
22. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
23. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
24. Speed bin (CL - tRCD - tRP) = 3 - 3 - 3
25. Speed bin (CL - tRCD - tRP) = 3 - 4 - 4 (all speed bins except DDR200)
26. tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms, if not already an integer, round to the next higher integer.
27. There must be at least two clock pulses during the tXSR period.
28. There must be at least one clock pulse during the tXP period.
29. t_{REFI} values are dependant on density and bus width.
30. A maximum of 8 Refresh commands can be posted to any given DDR, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*t_{REFI}.

Package Diagram

60-BALL 0.8mm pitch BGA





DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.20
A1	0.30	0.35	0.40
A2	–	–	0.84
A3	0.10	0.15	0.20
b	0.40	0.45	0.50
D	9.90	10.00	10.10
D1		7.20 BSC	
E	7.90	8.00	8.10
E1		6.40 BSC	
eE		0.80 BSC	
eD		0.80 BSC	
F		2.00 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.10
ddd	–	–	0.15
eee	–	–	0.08

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