May. 2020

SCQ16GN13AF1C-26V

288-Pin Nonvolatile Registered DDR4 SDRAM Modules
EU RoHS Compliant

Data Sheet

Rev. C

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2019-03	A	Initial Release
2019-11	B	Update PN and some description
2020-05	C	Update some description

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Contents

1 Overview

This chapter gives an overview of the 288-pin Nonvolatile Registered DDR4 SDRAM modules product family and describes its main characteristics.

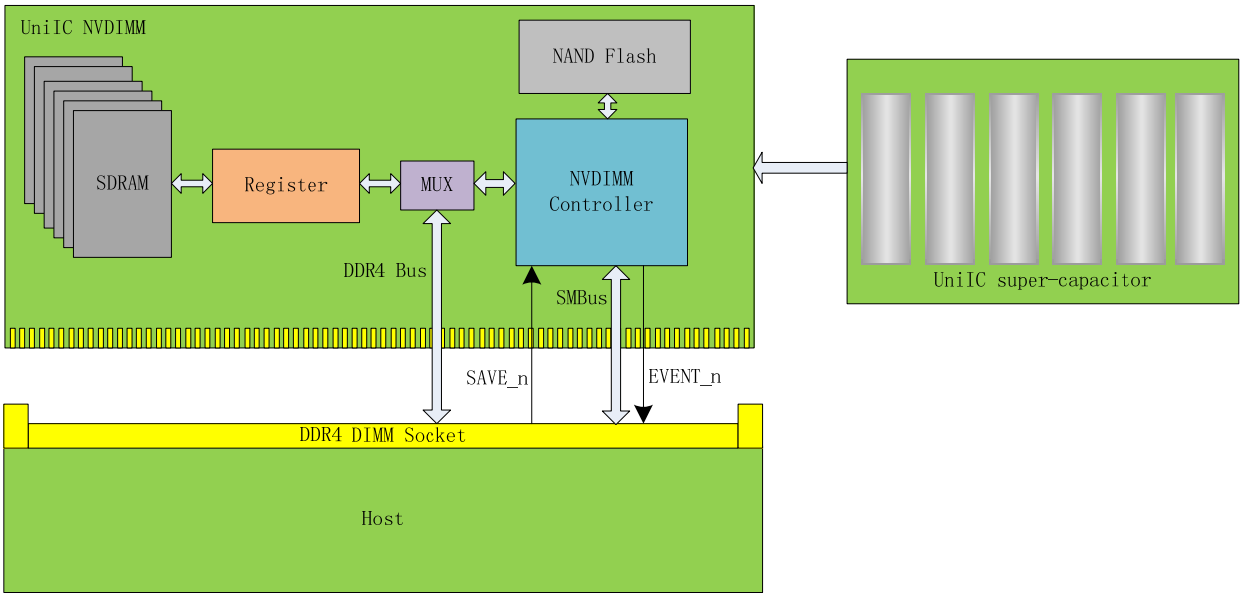
1.1 Features

- 288-Pin PC4-2666 Nonvolatile Registered DDR4 SDRAM memory modules
  DDR4 RDIMM, NAND Flash and super-capacitor management integrated in single module
  Power consumption for module: 2~5w
  Time cost for save operation: 55s
  ROHS
- 64GB SLC NAND Flash
  ONFI3.2
  72-bit BCH ECC per 1024B
- Persistent energy source options
  Option 1: Battery-free power source (super-capacitor)
  Option 2: Persistent DDR4 12V pin
- 1GB (2 Gig x 72) DDR4 RDIMM
- Fast data transfer rates: PC4-2400, PC4-2666
- Dual rank 16GB (2048M x 72) module organization, by 18pcs 1024M x 8 chips organization.
- VDD = 1.2V ±60mV
- VPP = 2.5V (2.375V~2.75V)
- VDDSPD = 2.5V
- Frequency/CAS latency
  0.75ns @ CL = 19 (DDR4-2666)
- Programmable CAS latency 9, 10,11, 12, 13, 14, 15 and 16, 17, 18,19 and 20 supported
- Programmable additive latency 0, CL-1, and CL-2 supported (x4/x8 only)
- Programmable CAS Write latency (CWL) = 9, 10, 11, 12, 14, 16,18
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Nominal and dynamic on-die termination (ODT) for strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die VREFDQ generation and calibration
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Average Refresh Cycle (Tcase of 0 °C ~ 95 °C)
  - 7.8 µs at 0 °C ~ 85 °C
  - 3.9 µs at 85 °C ~ 95 °C
- Multiple backup trigger methods
  ADR, SAVE_n assert
  SMBus command
- SuperCap Operation life
  5-year operating life
  0°C to 55°C operating range

1.2 Description

The UniIC NVDIMM is available as a JEDEC standard compatible with JESD245B.01 288-pin DDR4 RDIMM, with a 72-bit wide data bus in DRx8 configuration using 8Gb DRAM components for a 16GB DRAM density. **Figure 1** shows the system-level block diagram. As the Figure shows, the UniIC DDR4 NVDIMM is comprised of NVDIMM module and super-capacitor connected by a cable.

Figure 1 - UniIC DDR4 NVDIMM System Block Diagram



UniIC NVDIMM is a standard RDIMM pin-out module contains all of the DDR4 memory components, NAND Flash, power management and NVDIMM controller that preserve host's data in the event of the power failure. The interface between the host and NVDIMM module complies with the JEDEC DDR4 DIMM interface standard.

UniIC super-capacitor can provide power to the UniIC NVDIMM during a backup, which is connected to the UniIC NVDIMM via a proprietary cable and connection, providing backup power as well as health monitoring features. At power interruption of host, the super-capacitor ensures continuity of power while the SDRAM contents are saved. When the SAVE_n operation completes, the UniIC NVDIMM shuts down and discharge back-up power of super-capacitor.

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 288-Pin Nonvolatile Registered DDR4 SDRAM DIMM is listed by function in **Table 1** (288 pins).

Table 1 - Pin Configuration NVDIMM (288 pin)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V	145	12V	39	VSS	183	DQ25	77	VTT	221	VTT	114	VSS	258	DQ47
2	VSS	146	VREFCA	40	DQS12_t/ TDQS12_t	184	VSS	KEY				115	DQ42	259	VSS
3	DQ4	147	VSS	41	DQS12_c/ TDQS12_c	185	DQS3_c	78	EVENT_n	222	PARITY	116	VSS	260	DQ43
4	VSS	148	DQ5	42	VSS	186	DQS3_t	79	A0	223	VDD	117	DQ52	261	VSS
5	DQ0	149	VSS	43	DQ30	187	VSS	80	VDD	224	BA1	118	VSS	262	DQ53
6	VSS	150	DQ1	44	VSS	188	DQ31	81	BA0	225	A10/AP	119	DQ48	263	VSS
7	DQS9_t/ TDQS9_t	151	VSS	45	DQ26	189	VSS	82	RAS_n/A16	226	VDD	120	VSS	264	DQ49
8	DQS09_c/ TDQS9_c	152	DQS0_c	46	VSS	190	DQ27	83	VDD	227	NC	121	DQS15_t/ TDQS15_t	265	VSS
9	VSS	153	DQS0_t	47	CB4	191	VSS	84	CS0_n	228	WE_n /A14	122	DQS15_c/ TDQS15_c	266	DQS6_c
10	DQ6	154	VSS	48	VSS	192	CB5	85	VDD	229	VDD	123	VSS	267	DQS6_t
11	VSS	155	DQ7	49	CB0	193	VSS	86	CAS_n /A15	230	SAVE_n	124	DQ54	268	VSS
12	DQ2	156	VSS	50	VSS	194	CB1	87	ODT0	231	VDD	125	VSS	269	DQ55
13	VSS	157	DQ3	51	DQS17_t/ TDQS17_t	195	VSS	88	VDD	232	A13	126	DQ50	270	VSS
14	DQ12	158	VSS	52	DQS17_c/ TDQS17_c	196	DQS8_c	89	CS1_n/ NC	233	VDD	127	VSS	271	DQ51
15	VSS	159	DQ13	53	VSS	197	DQS8_t	90	VDD	234	A17	128	DQ60	272	VSS
16	DQ8	160	VSS	54	CB6	198	VSS	91	ODT1/ NC	235	NC/ C2	129	VSS	273	DQ61
17	VSS	161	DQ9	55	VSS	199	CB7	92	VDD	236	VDD	130	DQ56	274	VSS
18	DQS10_t/ TDQS10_t	162	VSS	56	CB2	200	VSS	93	CS2_n/ C0	237	CS3_n/ C1, NC	131	VSS	275	DQ57
19	DQS10_c/ TDQS10_c	163	DQS1_c	57	VSS	201	CB3	94	VSS	238	SA2	132	DQS16_t/ TDQS16_t	276	VSS
20	VSS	164	DQS1_t	58	RESET_n	202	VSS	95	DQ36	239	VSS	133	DQS16_c/ TDQS16_c	277	DQS7_c
21	DQ14	165	VSS	59	VDD	203	CKE1/ NC	96	VSS	240	DQ37	134	VSS	278	DQS7_t
22	VSS	166	DQ15	60	CKE0	204	VDD	97	DQ32	241	VSS	135	DQ62	279	VSS
23	DQ10	167	VSS	61	VDD	205	NC	98	VSS	242	DQ33	136	VSS	280	DQ63
24	VSS	168	DQ11	62	ACT_n	206	VDD	99	DQS13_t/ TDQ13_t	243	VSS	137	DQ58	281	VSS
25	DQ20	169	VSS	63	BG0	207	BG1	100	DQS13_c/ TDQS13_c	244	DQS4_c	138	VSS	282	DQ59
26	VSS	170	DQ21	64	VDD	208	ALERT_n	101	VSS	245	DQS4_t	139	SA0	283	VSS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
27	DQ16	171	VSS	65	A12 /BC_n	209	VDD	102	DQ38	246	VSS	140	SA1	284	VDDSPD
28	VSS	172	DQ17	66	A9	210	A11	103	VSS	247	DQ39	141	SCL	285	SDA
29	DQS11_t/ TDQS11_t	173	VSS	67	VDD	211	A7	104	DQ34	248	VSS	142	VPP	286	VPP
30	DQS11_c/ TDQS11_c	174	DQS2_c	68	A8	212	VDD	105	VSS	249	DQ35	143	VPP	287	VPP
31	VSS	175	DQS2_t	69	A6	213	A5	106	DQ44	250	VSS	144	NC	288	VPP
32	DQ22	176	VSS	70	VDD	214	A4	107	VSS	251	DQ45				
33	VSS	177	DQ23	71	A3	215	VDD	108	DQ40	252	VSS				
34	DQ18	178	VSS	72	A1	216	A2	109	VSS	253	DQ41				
35	VSS	179	DQ19	73	VDD	217	VDD	110	DQS14_t/ TDQS14_t	254	VSS				
36	DQ28	180	VSS	74	CK0_t	218	CK1_t	111	DQS14_c/ TDQS14_c	255	DQS5_c				
37	VSS	181	DQ29	75	CK0_c	219	CK1_c	112	VSS	256	DQS5_t				
38	DQ24	182	VSS	76	VDD	220	VDD	113	DQ46	257	VSS				

2.2 Pin Description

Table 2 - Pin Description

Pin Name	Description	Pin Name	Description
A0-A17	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I2C slave address select for SPD/TS and register
RAS_n	Register row address strobe input	PAR	Register parity input
CAS_n	Register column address strobe input	VDD	SDRAM core power supply
WE_n	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0-DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0-CB7	DIMM ECC check bits	EVENT_n	Interrupt signal for NVDIMM event to host
DQS0_t- DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c_ DQS17_c	Data Buffer data strobes (negative line of differential pair)	SAVE_n	Host interrupt signal to module for data save
CK0_t, CK1_t	Register clock input (positive line of differential pair)	12V	12V power supply
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

2.3 I/O Functional Description

Table 3 - Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	**Chip Select:** All commands are masked when CS-n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	**Chip ID :** Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	**On Die Termination:** ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	**Activation Command Input:** ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS n/A15. WE_n/A14	Input	**Command Inputs:** RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BG0 - BG1	Input	**Bank Group Inputs:** BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	**Bank Address Inputs:** BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.

Symbol	Type	Function
A0 - A17	Input	**Address Inputs:** Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16Gb x4 SDRAM configurations.
A10 / AP	Input	**Auto-precharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC_n	Input	**Burst Chop:** A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS	**Active Low Asynchronous Reset:** Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR	Input	**Command and Address Parity Input:** DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output (Input)	**Alert:** It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system. If the SDRAM ALERT_n pins are not connected to the ALERT_n pin on the edge connector is must still be connected to VDD on DIMM.
12V	Supply	**Power supply for charging NVDIMM backup energy storage device (PowerGEM)**: 12V±1.8V. Normal operation can be supported down to 6V; however, if these pins are being used to charge a super- capacitor, the charge time will be extended. Alternatively,these pins can be a persistent power supply for NVDIMM during SAVE operation: 6Vto 13.8V.
SAVE_n	Input (open drain)	**Force Save**: Active LOW, open-drain input pulled up to 2.5V through a 2K resistor. Commands the UniIC NVDIMM to switch its internal MUXs and copy the data in theSDRAM to internal NAND Flash. The SDRAM must be placed in self refresh mode beforeasserting this pin to ensure that no data is lost during this operation.
EVENT_n	Output	**Event notify**: Active LOW, when NVDIMM occurs warnings or important event pulled down to notify host
NC		**No Connect:** No on DIMM electrical connection is present

3 General Description

3.1 General Description

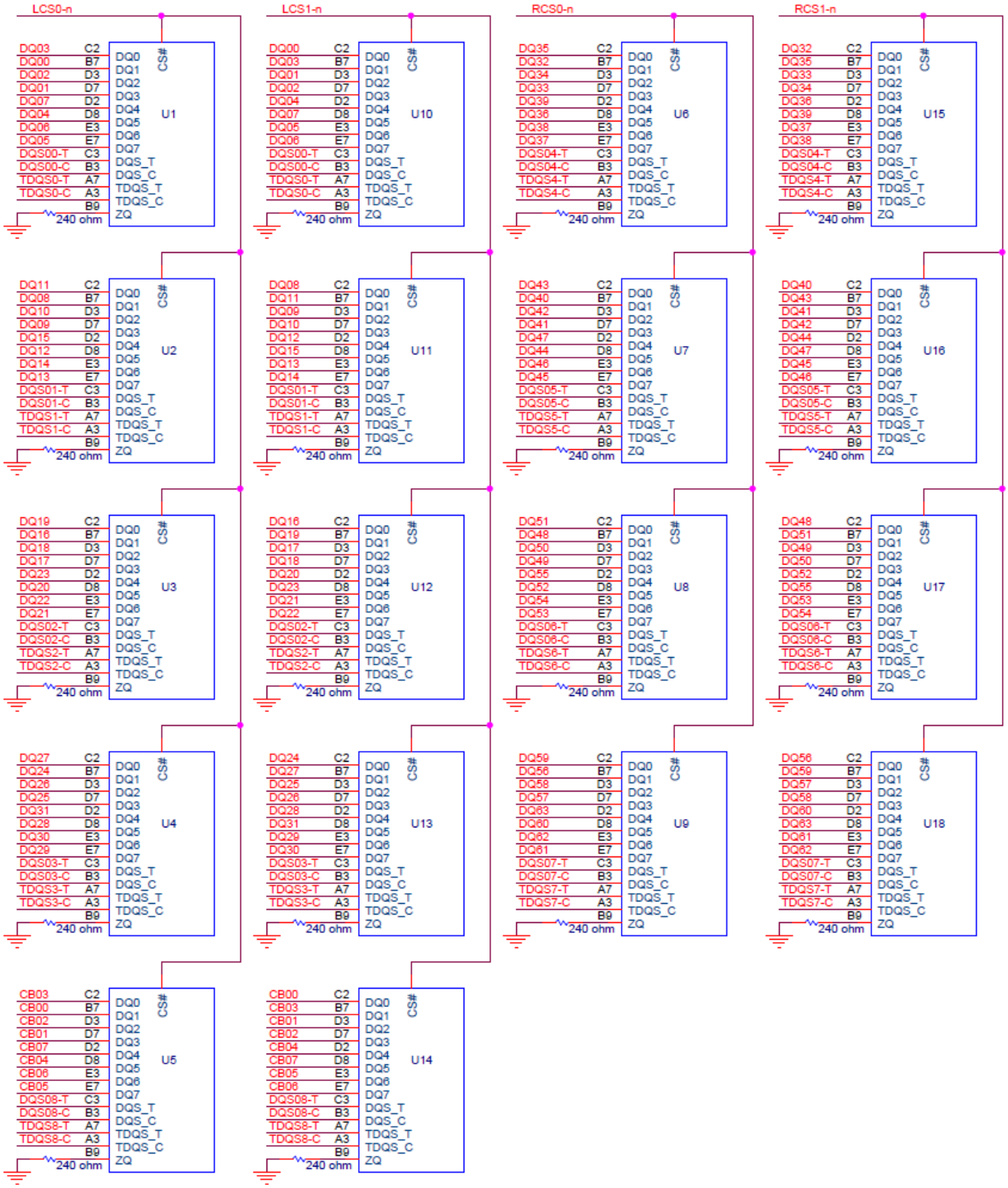
UniIC NVDIMM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. The modules utilizing 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing 16 banks. DDR4 SDRAM components use 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single operation of READ or WRITE for the DDR4 SDRAM consists of a single 8n-bit-wide effectively, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.
Two sets of differential signals are used: DQS and DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Using differential clocks and data strobes is to be ensured exceptional noise immunity for these signals and provide precise crossing points to capture the input signals.

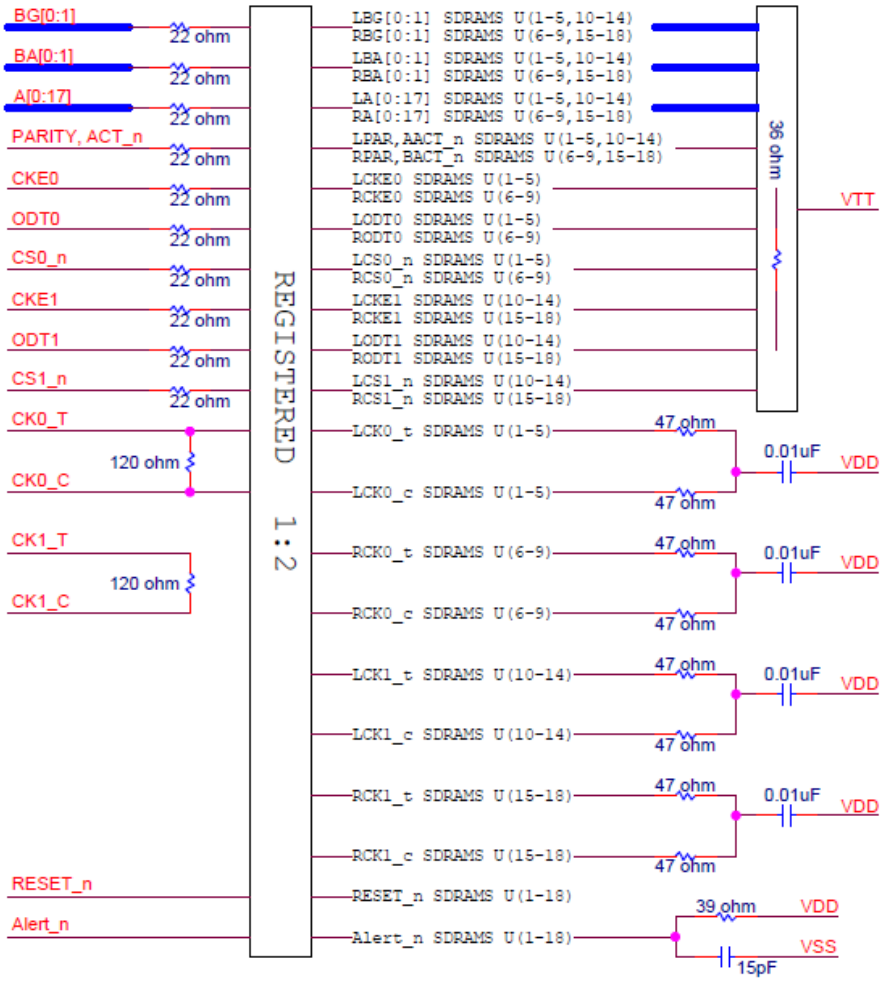
3.2 Serial Presence-Detect EEPROM Operation

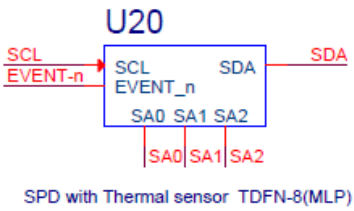
UniIC NVDIMM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus protpcol using the DIMM's SCL (clock) SDA (data), and SA (address) pins. The operation of write protect (WP) is connected to VSS, permanently disabling hardware write protection.

3.3 Function Block Diagram

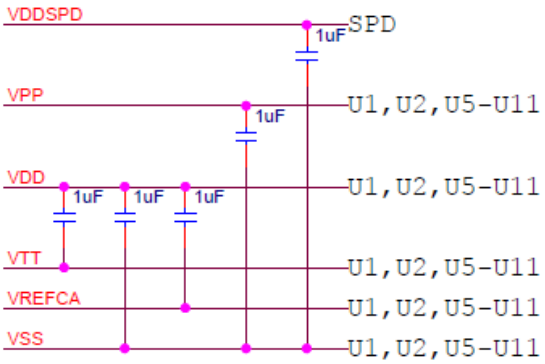
Figure 2 - NVDIMM Function Block Diagram

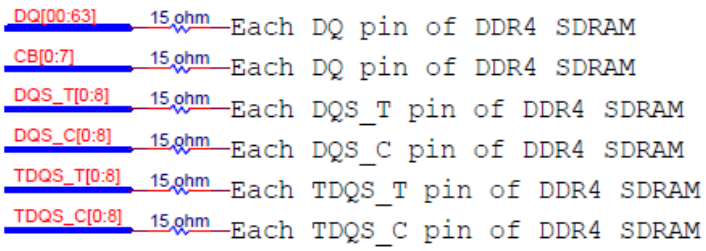






SPD with Thermal sensor TDFN-8(MLP)





3.4 DQ Map

Table 4 - DQ Map Rank0

Module Pin No.	Module DQ	Damping RES.	IC NO.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC NO.	IC DQ
5	0	R2	U15	0	16	8	R32	U16	0
150	1	R4		1	161	9	R36		1
12	2	R7		2	23	10	R38		2
157	3	R10		3	168	11	R41		3
3	4	R13		4	14	12	R44		4
148	5	R16		5	159	13	R46		5
10	6	R19		6	21	14	R49		6
155	7	R22		7	166	15	R54		7
27	16	R63	U17	0	38	24	R3	U18	0
172	17	R66		1	183	25	R5		1
34	18	R69		2	45	26	R8		2
179	19	R72		3	190	27	R11		3
25	20	R75		4	36	28	R14		4
170	21	R78		5	181	29	R17		5
32	22	R81		6	43	30	R20		6
177	23	R84		7	188	31	R23		7
49	CB0	R65	U19	0	97	32	R33	U20	0
194	CB1	R68		1	242	33	R34		1
56	CB2	R71		2	104	34	R39		2
201	CB3	R74		3	249	35	R42		3
47	CB4	R77		4	95	36	R45		4
192	CB5	R80		5	240	37	R47		5
54	CB6	R83		6	102	38	R50		6
199	CB7	R85		7	247	39	R52		7
108	40	R62	U21	0	119	48	R6	U23	0
253	41	R64		1	264	49	R9		1
115	42	R67		2	126	50	R12		2
260	43	R70		3	271	51	R15		3
106	44	R73		4	117	52	R18		4
251	45	R76		5	262	53	R21		5
113	46	R79		6	124	54	R24		6
258	47	R82		7	269	55	R25		7
130	56	R35	U22	0					
275	57	R37		1					
137	58	R40		2					
282	59	R43		3					
128	60	R48		4					
273	61	R51		5					
135	62	R53		6					
280	63	R55		7					

Table 5 - DQ Map Rank1

Module Pin No.	Module DQ	Damping RES.	IC NO.	IC DQ	Module Pin No.	Module DQ	Damping RES.	IC NO.	IC DQ
5	0	R2	U24	0	16	8	R32	U25	0
150	1	R4		1	161	9	R36		1
12	2	R7		2	23	10	R38		2
157	3	R10		3	168	11	R41		3
3	4	R13		4	14	12	R44		4
148	5	R16		5	159	13	R46		5
10	6	R19		6	21	14	R49		6
155	7	R22		7	166	15	R54		7
27	16	R63	U26	0	38	24	R3	U27	0
172	17	R66		1	183	25	R5		1
34	18	R69		2	45	26	R8		2
179	19	R72		3	190	27	R11		3
25	20	R75		4	36	28	R14		4
170	21	R78		5	181	29	R17		5
32	22	R81		6	43	30	R20		6
177	23	R84		7	188	31	R23		7
49	CB0	R65	U28	0	97	32	R33	U29	0
194	CB1	R68		1	242	33	R34		1
56	CB2	R71		2	104	34	R39		2
201	CB3	R74		3	249	35	R42		3
47	CB4	R77		4	95	36	R45		4
192	CB5	R80		5	240	37	R47		5
54	CB6	R83		6	102	38	R50		6
199	CB7	R85		7	247	39	R52		7
108	40	R62	U30	0	119	48	R6	U31	0
253	41	R64		1	264	49	R9		1
115	42	R67		2	126	50	R12		2
260	43	R70		3	271	51	R15		3
106	44	R73		4	117	52	R18		4
251	45	R76		5	262	53	R21		5
113	46	R79		6	124	54	R24		6
258	47	R82		7	269	55	R25		7
130	56	R35	U32	0					
275	57	R37		1					
137	58	R40		2					
282	59	R43		3					
128	60	R48		4					
273	61	R51		5					
135	62	R53		6					
280	63	R55		7					

4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

4.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6 - Absolute maximum ratings of the related voltage

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.4	+1.5	V	
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.4	+1.5	V	
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.4	3.0	V	
$12V$	Voltage on 12V pin relative to V_{SS}	-0.4	13.8	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.5	V	

Attention: Stresses above the max values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Table 7 - NVDIMM module environmental requirements

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+55	°C	
Storage Temperature	T_{STG}	– 50	+100	°C	
Barometric Pressure (operating & storage)	P_{Bar}	+69	+105	kPa	1)

1) Up to 3000m.

Table 8 - DRAM component operating temperature range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

4.2 Operating Conditions

Table 9 - Supply voltage levels and AC/DC operating conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.14	1.2	1.26	V	1),2),3)
Output Supply Voltage	V_{DDQ}	1.14	1.2	1.26	V	1),2),3)
Peak-to-Peak Voltage	V_{PP}	2.375	2.5	2.75	V	3)
Auxiliary NVDIMM Power Supply	$12V$	6	12	13.8	V	
Input Reference Voltage	V_{REF}	$0.49 \times V_{DD}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DD}$	V	
DC Input Logic High	$V_{IH.CA(DC75)}$	V_{REFCA} + 0.075	—	V_{DD}	V	
DC Input Logic Low	$V_{IL.CA\ (DC75)}$)	Vss	—	V_{REFCA} – 0.075	V	
AC Input Logic High	$V_{IH.CA(AC100)}$	V_{REF} + 0.1	—		V	
AC Input Logic Low	$V_{IL.CA\ (AC100)}$)		—	V_{REF} –0.1	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	

Notes:

1) Under all conditions VDDQ must be less than or equal to VDD.

2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3) DC bandwidth is limited to 20MHz.

4.3 Module and Component Speed Grades

Table 10 - NVDIMM module and DRAM component speed grades

Module Speed Grade	Component Speed Grade
-26V	2666MTs

4.4 I_{DD} Specifications and Conditions

Table 11 - I_{DD} Specifications

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0

Table 12 - I_{DD} Measurement Conditions

Symbol	Description
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[2]; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Dat asheet for detail pattern
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD6N	Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL
IDD6N	Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL

Symbol	Description
IDD6R	Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced[4]; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD6A	Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto[4]; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8	Maximum Power Down Current TBD

Notes :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].

2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK disable - set MR5 [A8:6 = 000]

3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]

4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature range 11] : Auto Self Refresh

Table 13 - I_{DD} Specification for UnilC NVDIMM Module

Product Type	SCQ16GN13AF1C-26V	Unit	Note[1)2)]
Organization	16GB		
	2 Rank (×8)		
	×72		
	-26V		
Symbol	Max.		
I_{DD0}	504	mA	3)
I_{DD1}	594	mA	3)
I_{DD2N}	486	mA	4)
I_{DD2NT}	450	mA	3)
I_{DD2P}	324	mA	4)
I_{DD2Q}	396	mA	4)
I_{DD3N}	810	mA	4)
I_{DD3P}	666	mA	4)
I_{DD4R}	1278	mA	3)
I_{DD4W}	1242	mA	3)
I_{DD5B}	1926	mA	3)
I_{DD6N}	396	mA	4)
I_{DD6E}	504	mA	4)
I_{DD6R}	252	mA	4)
I_{DD6A}	504	mA	4)
I_{DD7}	1530	mA	3)
I_{DD8}	216	mA	4)

1) Calculated values from component data.

2) $I_{DDX\ (rank)}$ = Number of components x $I_{DDX\ (component)}$

3) $I_{DDX} = I_{DDX\ (rank)} + (Rank-1) * I_{DD2P\ (rank)}$

4) I_{DDX} = Rank * $I_{DDX\ (rank)}$

5 Package Dimensions

Figure 3 - 288-pin DDR4 NVDIMM front and back view

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Xi'an: 4th Floor, Building A,
No. 38 Gaoxin 6th Road,
Xian High-tech Industries Development Zone
Xi'an, Shaanxi 710075, P. R. China
Tel: +86-29-88318000
Fax: +86-29-88453299

info@unisemicon.com

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