Dec. 2023

SCA32GR13H1F1C-56B

288-Pin DDR5 EC8 Registered DIMM(X80,ECC)

EU RoHS Compliant

Data Sheet

Rev. B

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2023-09	A	Initial Release
2023-12	B	Optimize the description

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1 Overview

This chapter gives an overview of the 288-pin DDR5 Registered DIMM product family and describes its main characteristics.

1.1 Features

- 288-Pin PC5-5600 DDR5 Registered DIMM
- Supports ECC error detection and correction
- On-DIMM SPD EEPROM with hub function and integrated temperature sensor (TS)
- On-DIMM Power management integrated circuit (PMIC)
- Two On-DIMM TS
- Frequency/CAS latency: 0.357ns @ CL = 46 (DDR5-5600)
- VDD = VDDQ = 1.1V
- VPP = 1.8V
- On-die, internal, adjustable VREF generation for DQ, CA, CS
- 32 internal banks: 8 groups of 4 banks each
- 16n-bit prefetch architecture
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated clock, control, command and address bus

Table 1 - Module Performance Table

UniIC Speed Code		**-56B**	**Unit**	**Note**
DRAM Speed Grade	**DDR5**	**-5600**		
CAS-RCD-RP latencies		**-46-45-45**	**t_{CK}**	
Min. RAS-CAS-Delay	t_{RCD}	16	ns	
Min. Row Precharge Time	t_{RP}	16	ns	
Min. Row Active Time	t_{RAS}	32	ns	
Min. Row Cycle Time	t_{RC}	48	ns	

1.2 Description

The UniIC 32GB module family are Registered DIMM with 31.25mm height based on DDR5 technology.

DIMMs intended for mounting into 288-pin connector sockets.

green Product

Table 2 - Ordering Information

Product Type	Compliance Code[1)]	Description	SDRAM Technology
PC5-5600 (46-45-45)			
SCA32GR13H1F1C-56B	32GB 2R×8 PC5-5600-46-45-45	2Ranks	16Gbit (×8)

1) This describes the speed grade, for example " PC5-5600-46-45-45" where 5600 means DIMM modules with 5600MT/s data rate and "46-45-45" means Column Address Strobe (CAS) latency=46, Row Column Delay (RCD) latency = 45 and Row Precharge (RP) latency = 45.

Table 3 - Address Format

DIMM Density	32GB(2Rx8,x80)
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	8 BG[2:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb(2Gx8)
Device Quantity	20

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 288-Pin Registered DIMM is listed by function in **Table 4** (288 pins).

Table 4 - Pin Configuration RDIMM (288 pin)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VIN_BULK	145	VIN_BULK	39	VSS	183	DQ23_A	76	CA0_B	220	RFU	114	VSS	258	DQ11_B
2	RFU	146	VIN_BULK	40	DQ24_A	184	VSS	77	VSS	221	CA1_B	115	DQS1_B_t	259	VSS
3	VIN_MGMT	147	PCAMP	41	VSS	185	DQ26_A	78	CA2_B	222	VSS	116	DQS1_B_c	260	DQS6_B_c, TDQS6_B_c
4	HSCL	148	HSA	42	DQ25_A	186	VSS	79	VSS	223	CA3_B	117	VSS	261	DQS6_B_t, TDQS6_B_t
5	HSDA	149	RFU	43	VSS	187	DQ27_A	80	CA4_B	224	VSS	118	DQ12_B	262	VSS
6	VSS	150	RFU	44	DQS3_A_t	188	VSS	81	VSS	225	CA5_B	119	VSS	263	DQ14_B
7	DQ0_A	151	VSS	45	DQS3_A_c	189	DQS8_A_c, TDQS8_A_c	82	CA6_B	226	VSS	120	DQ13_B	264	VSS
8	VSS	152	DQ2_A	46	VSS	190	DQS8_A_t, TDQS8_A_t	83	VSS	227	PAR_B	121	VSS	265	DQ15_B
9	DQ1_A	153	VSS	47	DQ28_A	191	VSS	84	CS0_B_n	228	VSS	122	DQ16_B	266	VSS
10	VSS	154	DQ3_A	48	VSS	192	DQ30_A	85	VSS	229	CS1_B_n	123	VSS	267	DQ18_B
11	DQS0_A_t	155	VSS	49	DQ29_A	193	VSS	86	LBDQ	230	VSS	124	DQ17_B	268	VSS
12	DQS0_A_c	156	DQS5_A_c, TDQS5_A_c	50	VSS	194	DQ31_A	87	LBDQS	231	RFU	125	VSS	269	DQ19_B
13	VSS	157	DQS5_A_t, TDQS5_A_t	51	CB0_A	195	VSS	88	VSS	232	RFU	126	DQS2_B_t	270	VSS
14	DQ4_A	158	VSS	52	VSS	196	CB2_A	89	CB4_B	233	VSS	127	DQS2_B_c	271	DQS7_B_c, TDQS7_B_c
15	VSS	159	DQ6_A	53	CB1_A	197	VSS	90	VSS	234	CB6_B	128	VSS	272	DQS7_B_t, TDQS7_B_t
16	DQ5_A	160	VSS	54	VSS	198	CB3_A	91	CB5_B	235	VSS	129	DQ20_B	273	VSS
17	VSS	161	DQ7_A	55	DQS4_A_t	199	VSS	92	VSS	236	CB7_B	130	VSS	274	DQ22_B
18	DQ8_A	162	VSS	56	DQS4_A_c	200	DQS9_A_c, TDQS9_A_c	93	DQS9_B_t, TDQS9_B_t	237	VSS	131	DQ21_B	275	VSS
19	VSS	163	DQ10_A	57	VSS	201	DQS9_A_t, TDQS9_A_t	94	DQS9_B_c, TDQS9_B_c	238	DQS4_B_c	132	VSS	276	DQ23_B
20	DQ9_A	164	VSS	58	CB4_A	202	VSS	95	VSS	239	DQS4_B_t	133	DQ24_B	277	VSS
21	VSS	165	DQ11_A	59	VSS	203	CB6_A	96	CB0_B	240	VSS	134	VSS	278	DQ26_B
22	DQS1_A_t	166	VSS	60	CB5_A	204	VSS	97	VSS	241	CB2_B	135	DQ25_B	279	VSS

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
23	DQS1_A_c	167	DQS6_A_c, TDQS6_A_c	61	VSS	205	CB7_A	98	CB1_B	242	VSS	136	VSS	280	DQ27_B
24	VSS	168	DQS6_A_t, TDQS6_A_t	62	ALERT_n	206	VSS	99	VSS	243	CB3_B	137	DQS3_B_t	281	VSS
25	DQ12_A	169	VSS	63	VSS	207	RESET_n	100	DQ0_B	244	VSS	138	DQS3_B_c	282	DQS8_B_c, TDQS8_B_c
26	VSS	170	DQ14_A	64	CS0_A_n	208	VSS	101	VSS	245	DQ2_B	139	VSS	283	DQS8_B_t, TDQS8_B_t
27	DQ13_A	171	VSS	65	VSS	209	CS1_A_n	102	DQ1_B	246	VSS	140	DQ28_B	284	VSS
28	VSS	172	DQ15_A	66	CA0_A	210	VSS	103	VSS	247	DQ3_B	141	VSS	285	DQ30_B
29	DQ16_A	173	VSS	67	VSS	211	CA1_A	104	DQS0_B_t	248	VSS	142	DQ29_B	286	VSS
30	VSS	174	DQ18_A	68	CA2_A	212	VSS	105	DQS0_B_c	249	DQS5_B_c, TDQS5_B_c	143	VSS	287	DQ31_B
31	DQ17_A	175	VSS	69	VSS	213	CA3_A	106	VSS	250	DQS5_B_t, TDQS5_B_t	144	RFU	288	VSS
32	VSS	176	DQ19_A	70	CA4_A	214	VSS	107	DQ4_B	251	VSS				
33	DQS2_A_t	177	VSS	71	VSS	215	CA5_A	108	VSS	252	DQ6_B				
34	DQS2_A_c	178	DQS7_A_c, TDQS7_A_c	72	CA6_A	216	VSS	109	DQ5_B	253	VSS				
35	VSS	179	DQS7_A_t, TDQS7_A_t	73	VSS	217	CK_t	110	VSS	254	DQ7_B				
36	DQ20_A	180	VSS	74	PAR_A	218	CK_c	111	DQ8_B	255	VSS				
37	VSS	181	DQ22_A	75	VSS	219	VSS	112	VSS	256	DQ10_B				
38	DQ21_A	182	VSS	KEY				113	DQ9_B	257	VSS				

2.2 Pin Descriptions

Table 5 – Pin Descriptions

Symbol	Type	I/O Level	Description
CK_t, CK_c	Input	VDDQ	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A CA[6:0]_B	DDR Input	VDDQ	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during MODE REGISTER SET commands.
CS[1:0]_A CS[1:0]_B	Input	VDDQ	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external rank selection on systems with multiple ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down mode and self refresh mode. While not in self refresh mode the CS_n input buffer operates with the same ODT and V_{REF} parameters as configured by the CA_ODT strap setting or mode register. When in self refresh, the CS_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDD.
PAR_A PAR_B	Input	VDDQ	Command and Address Parity Input: The RCD supports even parity check devices prior to forwarding commands to the DRAM. Once enabled on the RCD, the RCD calculates parity. Input parity should be maintained at the rising edge of the clock and at the same time with command and address with CSx- _x_n LOW.
ALERT_n	Output	VDDQ	Alert: If there is an error in CRC, then ALERT_n drives LOW for the period time interval and returns HIGH. During connectivity test mode, this pin functions as an input. Usage of this signal is system-dependent. In the case where this pin is not connected, ALERT_n must be bonded to V_{DDQ} on the system board.
RESET_n	CMOS Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail-to-rail signal with DC HIGH and LOW at 80% and 20% of VDDQ.
PCAMP	Input/Output	VDDQ	Control and Monitor Port: Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_-GOOD).
HSCL	Input	VOUT_1.0V	Host Sideband Bus Clock: Bus clock used to strobe data into HUB device. When open drain, a pull-up resistor is required on the system motherboard.
HSDA	Input/Output	VOUT_1.0V	Host Sideband Bus Data: I2C/I3C-Basic data. When open drain, a pull-up resistor is required on the system motherboard.
HSA	Input	GND	Host Sideband Bus Device ID: Address input to a hub or other client device to distinguish between identical devices in the I3C basic address range. Tied to GND, HSA has different resistor values on the motherboard to identify DIMM slot address. Refer to the SPD Hub spec for more information.

Symbol	Type	I/O Level	Description
DQ[31:0]_A DQ[31:0]_B	Input/Output	VDDQ	Data Input/Output: Bidirectional data bus. If CRC is enabled via the mode register, then CRC code is added at the end of data burst. Any DQ from DQ0—DQ3 may indicate the internal V_{REF} level during test via mode register setting MR4 A4 = HIGH. Refer to the vendor-specific data sheets to determine which DQ is used.
CB[7:0]_A CB[7:0]_B	Input/Output	VDDQ	ECC Check Bits Input/Output: Bidirectional data bus.
DQS[9:0]_A_t DQS[9:0]_B_t DQS[9:0]_A_c DQS[9:0]_B_c	Input/Output	VDDQ	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM only supports differential data strobe. It does not support single-ended strobe.
TDQS[9:0]_A_t TDQS[9:0]_B_t TDQS[9:0]_A_c TDQS[9:0]_B_c	Input/Output	VDDQ	Termination Data Strobe: Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.
LBDQ	Output	VDDQ	Loopback data output: The output of this device on the loopback output select defined in MR53:0P[4:0]. When loopback is enabled, it is in driver mode using the default RON described in the loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
LBDQS	Output	VDDQ	Loopback data strobe output: This is a single-ended strobe with the rising edge aligned with loopback data edge, falling edge aligned with data center. When loopback is enabled, it is in driver mode using the default Ron described in the loopback function section. When loopback is disabled, the pin is either terminated or High-Z based on MR36:OP[2:0].
VIN_BULK	Supply		External Power Supply: 12V, 4.25V (min), 15V (max)
VIN_MGMT	Supply		External Power Supply: 3.3V, 3.0V (min), 3.6V (max)
VSS	Supply		Ground
RFU			Reserved for future use. No on DIMM electrical connection is present.
NC			No connect: No internal electrical connection is present.
NF			No function: May have internal connection present, but has no function.

3 General Description

3.1 General Description

High-speed DDR5 SDRAM modules use DDR5 SDRAM devices with four or eight internal memory bank groups. DDR5 SDRAM devices have eight internal bank groups consisting of four memory banks each, providing a total of 32 banks. DDR5 SDRAM modules benefit from DDR5 SDRAM's use of a 16n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR5 SDRAM effectively consists of a single 16n-bit-wide, eight-clock data transfer at the internal DRAM core and sixteen corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.
DDR5 modules use two sets of differential signals (DQS_t and DQS_c) to capture data, and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

3.2 Registering Clock Driver Operation

DDR5 RDIMM has a registering clock driver (RCD) consisting of a register and a phase-lock loop (PLL).
(The device complies with the JEDEC DDR5 RCD specification (JESD82-511 (DDR5RCD01))
RCD has several functions including reducing the electrical load on the host memory controller's command, address, and control bus, redriving signals to the DDR5 SDRAM devices for increasing signal integrity, and providing a low-jitter, low-skew PLL that redistributes a differential clock pair to multiple differential pairs of clock outputs.
The RCD also has a parity-checking function. By default, when device is put in I3C-basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. The RCD receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified command/address inputs; it indicates on its open-drain ALERT_n pin whether a parity error has occurred. If parity checking is enabled, the RCD forwards commands to the SDRAM when no parity error has occurred. If the parity error function is disabled, the RCD forwards sampled commands to the SDRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled. Parity is checked separately on the two sub-channels for both 1UI and 2UI command. A parity error on one sub-channel does not affect the operation of the other sub-channel.

3.3 Power Management Integrated Circuit Operation

The power management integrated circuit (PMIC) is new for DDR5. This operation converts a 12V supply into regulated values for components on the module. For RDIMMs, there are two devices defined within JEDEC: the PMIC5000 (high output power) and PMIC5010 (low output power) for different usage. The PMIC allows the host to monitor voltage and current via the sideband channel (Refer to the PMIC5000, PMIC5010 JEDEC specification for full details).

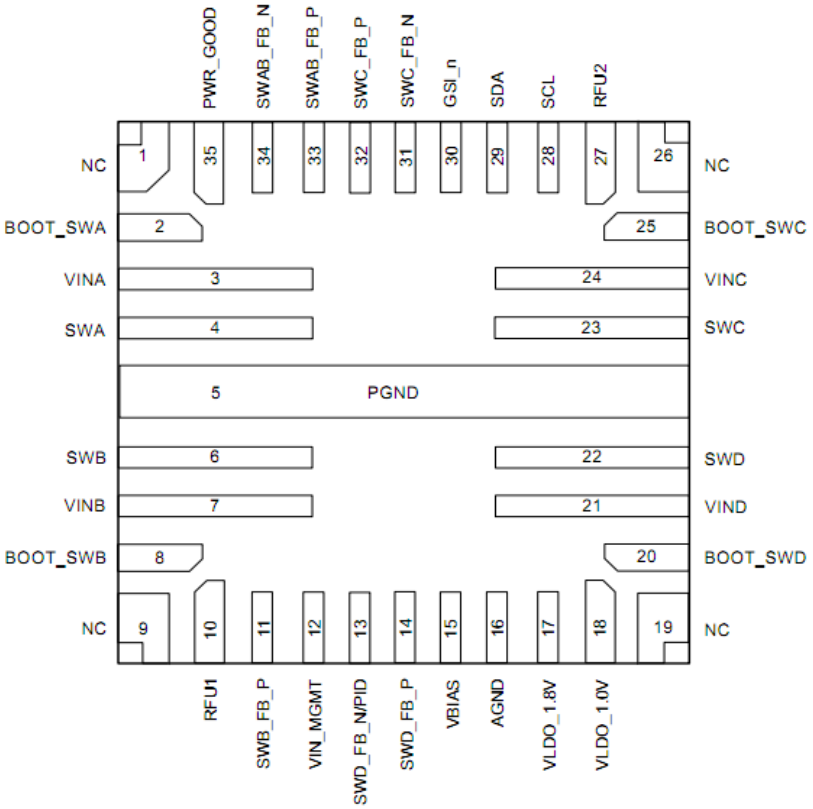
The PMIC has two supply inputs, a 3.3V VIN_Mgmt supply and the 12V nominal supply from the card edge through VIN_BULK. The VIN_Mgmt is used to generate the internal bias voltage for reading operation from its internal non-volatile memory content and to generate LDO voltages.

The VIN_BULK supply is used by the PMIC for all buck regulators.

By default, the PMIC powers up in I2C mode, and the host can reconfigure to support I3C-basic if needed. Please see the address configuration as below table for the PMIC Address ID (PID), device pin #13.

Table 6 – PMIC Addressing

PID Configuration (Pin #13)	PMIC Address ID (PID)			
	Bit 7	Bit 6	Bit 5	Bit 4
Pin to Vss	1	0	0	1



3.4 Temperature Sensor Operation

Temperature sensor devices incorporate thermal sensing capability which is controlled and read over two-wire bus. TS device operate from a nominal 1.8V nominal power supply (V_{DDSPD}) and a 1.0V nominal power supply (V_{DDIO}). TS device is intended to operate up to 12.5 MHz on a 1.0V I3C-basic bus or up to 1 MHz on a 1.0V to 3.3 V (Grade dependent) I2C bus. TS device is intended to interface to I2C or I3C-basic buses which have multiple devices on a shared bus, and must be uniquely addressed with fixed addressing on the same bus (Refer to the JEDEC JESD302-1 TS511x specification for more details).

3.5 SPD EEPROM HUB Operation

DDR5 SDRAM modules incorporate an SPD EEPROM with hub function with integrated thermal sensor (TS). The SPD data is stored in a 1024-byte including16 blocks (64 bytes per block), and each block may optionally be write-protected via software command.

The EEPROM resides on a two-wire I3C serial interface, which is also compatible with legacy I2C interface and is not integrated with the memory bus in any manner. It operates as an initiator/target device in the I3C-basic protocol, with all operations synchronized by the serial clock. Transfer rates of up to 12.5 MHz are achievable at 1.0V (NOM).

The first 640 bytes are programmed by UniIC for DIMM parameters related usage. The remaining 384 bytes are available for the end user.

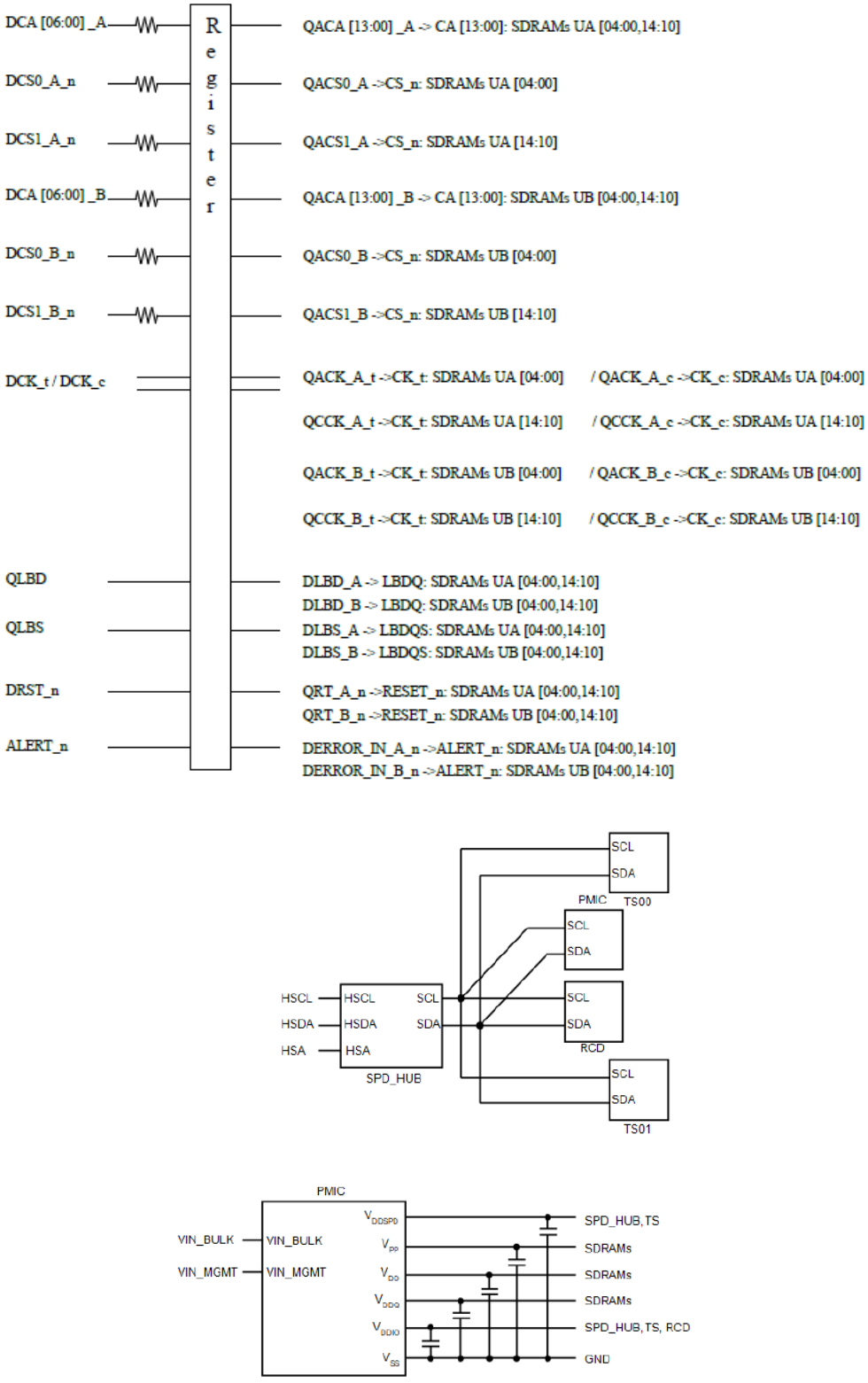
UniIC implements reversible software write protection on DDR5 SDRAM-based modules. This prevents the lower 640 bytes (bytes 0 to 639) from being inadvertently programmed or corrupted. The upper 384 bytes remain available for customer use and are unprotected.

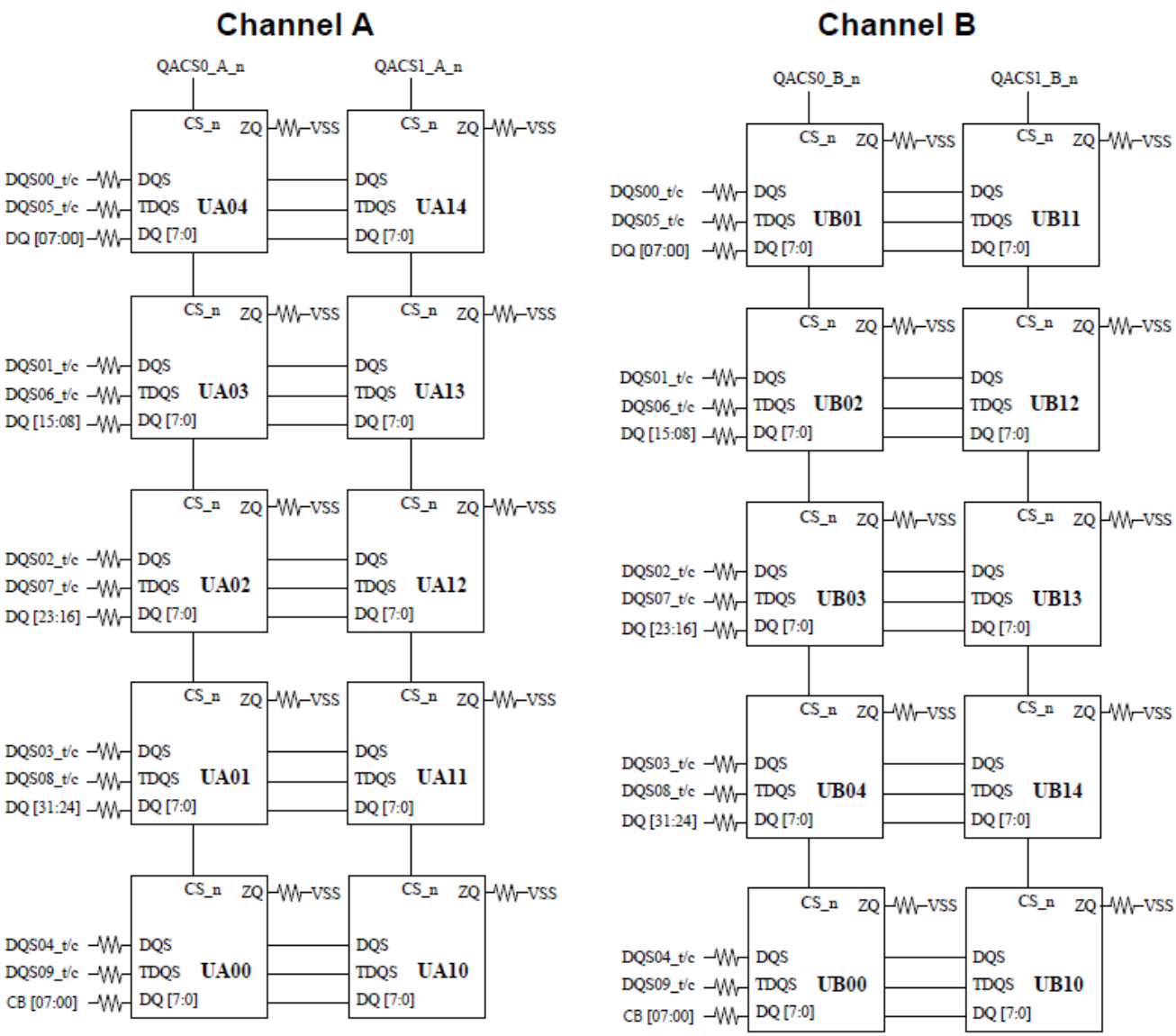
Table 7 – SPD Byte Information

Block	Range		Description
0	0~63	0x000~0x03F	Base configuration and DRAM parameters
1	64~127	0x040~0x07F	Base configuration and DRAM parameters
2	128~191	0x080~0x0BF	Reserved for future use
3	192~239	0x0C0~0x0EF	Common Module Parameters -- See annex A.0 for details
	240~255	0x0D0~0x0FF	Standard module parameters -- See annexes A.x for details
4	256~319	0x100~0x13F	Standard module parameters -- See annexes A.x for details
5	320~383	0x140~0x17F	Standard module parameters -- See annexes A.x for details
6	384~447	0x180~0x1BF	Standard module parameters -- See annexes A.x for details
7	448~509	0x1C0~0x1FF	Reserved for future use
	510~511	0x1FE~0x1FF	CRC for SPD bytes 0~509
8	512~575	0x200~0x23F	Manufacturing information
9	576~639	0x240~0x27F	Manufacturing information
10	640~703	0x280~0x2BF	End user programmable
11	704~767	0x2C0~0x2FF	End user programmable
12	768~831	0x300~0x33F	End user programmable
13	832~895	0x340~0x37F	End user programmable
14	896~959	0x380~0x3BF	End user programmable
15	960~1023	0x3C0~0x3FF	End user programmable

3.6 Function Block Diagram

Figure 1 - Function Block Diagram_SCA32GR13H1F1C-56B





Note 1: Unless otherwise noted resistors are 15 Ω ± 5%

Note 2: ZQ resistors are 240 Ω ± 1%.

3.7 DQ Map

Table 8 - DQ Map _ SCA32GR13H1F1C-56B

Module Pin NO.	Module DQ NO.	Damping RES.	R0 IC NO.	R0 IC DQ	R1 IC NO.	R1 IC DQ	Module Pin NO.	Module DQ NO.	Damping RES.	R0 IC NO.	R0 IC DQ	R1 IC NO.	R1 IC DQ
7	0_A	R061	UA04	1	UA14	0	18	8_A	R029	UA03	1	UA13	0
9	1_A	R062		2		3	20	9_A	R030		2		3
152	2_A	R064		3		2	163	10_A	R032		3		2
154	3_A	R063		0		1	165	11_A	R031		0		1
14	4_A	R065		5		4	25	12_A	R033		5		4
16	5_A	R066		6		7	27	13_A	R034		6		7
159	6_A	R028		7		6	170	14_A	R036		7		6
161	7_A	R027		4		5	172	15_A	R035		4		5
29	16_A	R037	UA02	1	UA12	0	40	24_A	R045	UA01	1	UA11	0
31	17_A	R038		2		3	42	25_A	R046		2		3
174	18_A	R040		3		2	185	26_A	R048		3		2
176	19_A	R039		0		1	187	27_A	R047		0		1
36	20_A	R041		5		4	47	28_A	R049		5		4
38	21_A	R042		6		7	49	29_A	R050		6		7
181	22_A	R044		7		6	192	30_A	R052		7		6
183	23_A	R043		4		5	194	31_A	R051		4		5
51	CB00_A	R053	UA00	1	UA10	0	100	0_B	R067	UB01	1	UB11	0
53	CB01_A	R054		2		3	102	1_B	R068		2		3
196	CB02_A	R056		3		2	245	2_B	R070		3		2
198	CB03_A	R055		0		1	247	3_B	R069		0		1
58	CB04_A	R057		5		4	107	4_B	R071		5		4
60	CB05_A	R058		6		7	109	5_B	R072		6		7
203	CB06_A	R060		7		6	252	6_B	R074		7		6
205	CB07_A	R059		4		5	254	7_B	R073		4		5
111	8_B	R075	UB02	1	UB12	0	122	16_B	R083	UB03	1	UB13	0
113	9_B	R076		2		3	124	17_B	R084		2		3
256	10_B	R078		3		2	267	18_B	R086		3		2
258	11_B	R077		0		1	269	19_B	R085		0		1
118	12_B	R079		5		4	129	20_B	R087		5		4
120	13_B	R080		6		7	131	21_B	R088		6		7
263	14_B	R082		7		6	274	22_B	R090		7		6
265	15_B	R081		4		5	276	23_B	R089		4		5
133	24_B	R091	UB04	1	UB14	0	96	CB00_B	R103	UB00	1	UB10	0
135	25_B	R092		2		3	98	CB01_B	R104		2		3
278	26_B	R094		3		2	241	CB02_B	R106		3		2
280	27_B	R093		0		1	243	CB03_B	R105		0		1
140	28_B	R095		5		4	89	CB04_B	R099		5		4
142	29_B	R096		6		7	91	CB05_B	R100		6		7
285	30_B	R098		7		6	234	CB06_B	R102		7		6
287	31_B	R097		4		5	236	CB07_B	R101		4		5

4 Electrical Characteristics

4.1 AC and DC Operation Conditions

Table 9 - Absolute Maximum DC Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.3	+1.4	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.3	+1.4	V	1)
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	-0.3	+2.1	V	3)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3	+1.4	V	1)
T_{STG}	Storage Temperature	-55	+100	℃	1),2)

Notes:

1) Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.

3) VPP must be equal or greater than VDD /VDDQ at all times during power on and operation of DRAM device.

Table 10 – DC Voltage Operating Conditions

Symbol	Parameter	Low Frequency Voltage Spec			Unit	Note
		Min.	Typ	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	1.067(-3%)	1.1	1.166(+6%)	V	1), 2)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	1.067(-3%)	1.1	1.166(+6%)	V	1), 2)
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	1.746(-3%)	1.8	1.908(+6%)	V	1), 2)

Notes:

1) VDD must be within 66mV of VDDQ.

2) AC parameters are measured with VDD and VDDQ tied together.

Table 11 - DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Grade	Note
		Min.	Max.			
T_{OPER_NORMAL}	Normal Operating Temperature	0	85	°C	NT	1),2),3),4)
$T_{OPER\_EXTENDED}$	Extended Operating Temperature	0	95	°C	XT	1),2),3),4)

Notes:

1) All operating temperature symbols, ranges, acronyms from JESD402-1.
2) Operating Temperature is the case surface temperature on the center / top side of the DRAM. For the measurement conditions, refer to JESD51-2.
3) All devices are required to operate in NT and XT temperature ranges.
4) When operating above 85°C, the host shall provide appropriate refresh mode controls associated with increased temperature range. The full description of these settings are defined in the tREFI parameters for REFab and REFsb command by device density table in the Refresh operations section (DRAM datasheet).

4.2 Module and Component Speed Grades

DDR5 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Table 12 - Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-56B	5600-46-45-45

4.3 I_{DD} Specifications and Conditions

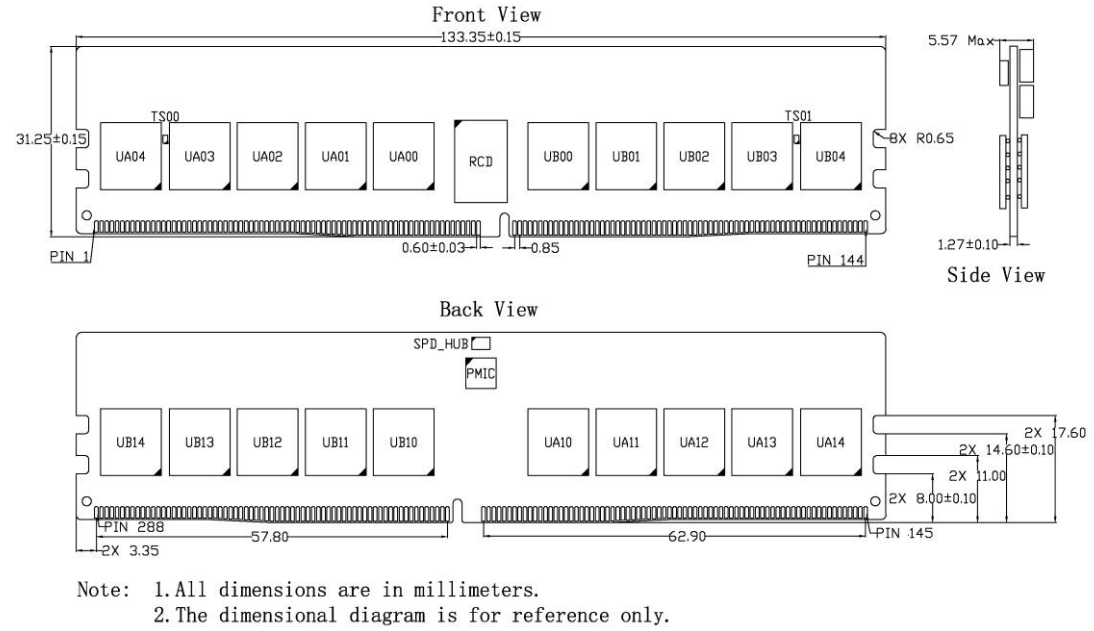
Table 13 - I_{DD} Specification for SCA32GR13H1F1C-56B

Module IDD is based on PMIC VIN_BULK 12V input current and typical operating temperature. Each IDD parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (VDD, VDDQ and VPP).

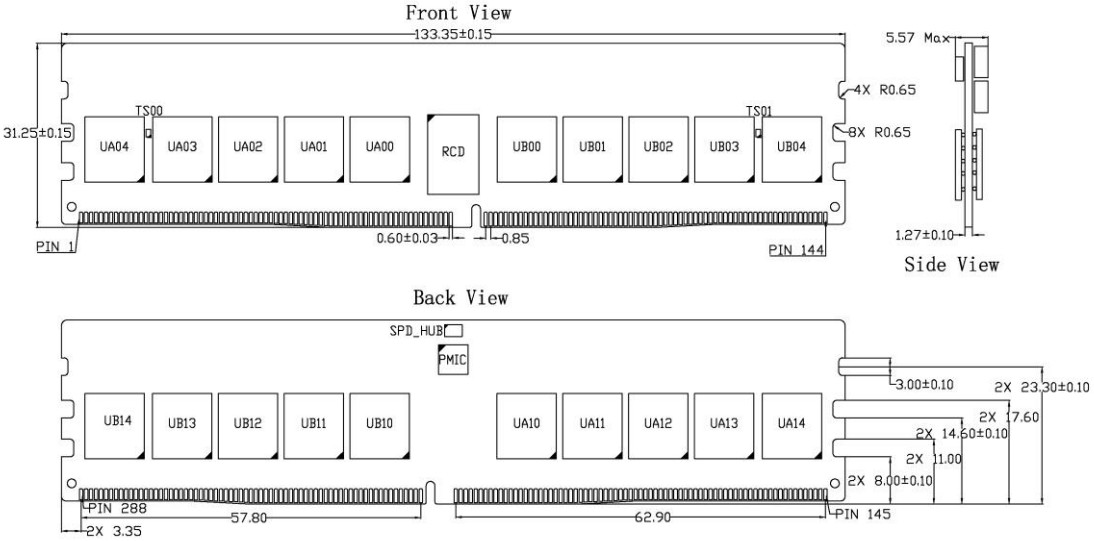
Product Type		SCA32GR13H1F1C-56B	Unit	Note
Organization		32GB		
		2Rank (×8)		
		×80		
		-56B		
Parameter	Symbol	Current		
Operating one bank ACTIVATE-PRECHARGE current	IDD0	185.9	mA	
Operating four bank ACTIVATE-PRECHARGE current	IDD0F	230.6	mA	
Precharge standby current	IDD2N	169.1	mA	
Precharge standby non-target command	IDD2NT	200.3	mA	
Precharge power-down current	IDD2P	156.8	mA	
Active standby current	IDD3N	231.5	mA	
Active power-down current	IDD3P	218.7	mA	
Operating burst read current	IDD4R	501.4	mA	
Operating burst write current	IDD4W	584.0	mA	
Burst refresh (normal refresh mode) current	IDD5B	406.6	mA	
Burst refresh (fine granularity refresh mode) current	IDD5F	390.8	mA	
Burst refresh (same bank refresh mode) current	IDD5C	267.3	mA	
Self refresh current	IDD6N	124.6	mA	
Operating bank interleave read current	IDD7	609.5	mA	
Maximum power saving deep power down mode current	IDD8	56.7	mA	

5 Package Dimensions

Figure 2 - Package Dimensions_SCA32GR13H1F1C-56B



Note: 1. All dimensions are in millimeters.
2. The dimensional diagram is for reference only.



Note: 1. All dimensions are in millimeters.
2. The dimensional diagram is for reference only.

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